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ANALOG-TO-DIGITAL CONVERSION TECHNIQUES FOR APPLICATION IN DIGITAL CONTROL SYSTEMS

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ANALOG-TO-DIGITAL CONVERSION TECHNIQUES FOR APPLICATION IN DIGITAL CONTROL SYSTEMS

by

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ABSTRACT

This thesis is primarily concerned with a comparative study of analog-to-digital conversion techniques as currently available. Those discussed and evaluated are of the electromechanical and electronic types including coded patterns, incremental devices, simultaneous, feedback encoding, and time base conversion. In addition to the study of converter techniques and characteristics the last section is devoted to a practical application for a turbine engine fuel control system. Numerous tables and charts for purposes of comparison are included.

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LIST OF SYMBOLS AND ABBREVIATIONS

ADC	Analog-to-Digital Converter
DAC	Digital-to-Analog Converter
A-D	Analog-to-Digital and Digital-to-Analog
BCD	Binary Coded Decimal
BIT	Binary Digit
mv	millivolt
us	microsecond
Ref	Reference
	AND gate
	OR gate
	Inverter

ACKNOWLEDGEMENT

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1. Introduction

In recent years great advances have been made in the technology of digital computers, particularly in their speed of operation and reliability. With the assurance of these factors it is now possible to include the digital computer within a control system. The increase in speed of operation of the digital computer has made it possible to time share the computer's function so that it can be used for several control functions simultaneously, thereby often making digital control economically feasible. The increase of computer reliability has reduced the necessity for backup analog systems in case of failure.

One of the major problems in using a digital computer in a control loop lies in the fact that the plant to be controlled operates in real time whereas the computer treats the time variable in a problem as a number. Thus the digital computer must perform its calculations fast enough so that the results are available in enough time to be of value in controlling the plant. Another way of looking at this problem is that the inclusion of a digital computer in a control system inherently makes the system sampled and the computer must function fast enough so that the basic sampling rate allows for smooth and continuous control. The digital computer operates on coded numbers whereas a plant operates with physical parameters such as shaft position, angular rotation, lateral motion, weight, volume, or pressure. Essentially the plant/computer interface must include an analog to digital encoding at the computer input and some form of digital to analog decoding at the computer output. This thesis is concerned primarily with the techniques for accomplishing analog to digital conversion and the characteristics of such devices. Additionally the last section is devoted to an application of these various techniques of analog to digital conversion in a fuel control system.

2. Converter Characteristics

There are two basic types of A-D converters.[1] These are the mechanical to electrical (called electromechanical) converters and the electrical to electrical (called electronic) converters.

In the electromechanical converter, a shaft position, shaft rotation, or translational motion is to be converted to a digital number. The electronic converter will transform a voltage to a digital number. Although these two types of converters seem different, their basic characteristics are the same. The characteristics that must be kept in mind for any practical application are:

(a) Basic sampling rate.

(b) Analog-to-Digital conversion time.

(c) Resolution and accuracy.

(d) Possible ambiguities in output data.

(e) Temporary storage or data holding characteristics.

(f) Adaptability for time multiplexing.

These characteristics are discussed in detail in the sections which follow.

A. Basic Sampling Rate:

Sampling rate is the basic repetition rate at which the analog signal is converted into digital data.

The technique for achieving the conversion must be capable of at least providing the minimum number of samples as specified by the sampling theorem [1] to prevent the loss of information. According to E. J. Sampson, [2] "in the practical situation one would have to sample at a much greater frequency to compensate for the non-ideal characteristics of physical

[1] Abbreviations used in this thesis are listed on page 5.

devices." Indeed this is the case and rates ranging from 10 to 20 times the sampling theorem rates have been used so that the computer controlled plant output is smooth and contains no granularity. [3]

B. Analog-to-Digital Conversion Time

Tou [4] defines conversion time "as the interval between the instant at which an input signal to be converted is applied to the conversion device and the instant at which the output signal has been established within desired accuracy." This is shown in figure 2.1 where the conversion time should normally be less than the repetition period unless a delay greater than the sampling period can be tolerated in the output. It is this conversion time that determines the converter's bandwidth rather than the number of sampling operations which can be performed in a given amount of time. [5] This can be best illustrated by the following example.

Example 2.1 [5] : What is the highest frequency that a serial output converter with a conversion speed of 4 microseconds per bit can sample to 10 bit accuracy?

Solution: For 10-bit accuracy, the input must not change more than one bit in the least significant place. The maximum change is then 2^{-10}. This change can occur in the length of time required to set 10 bits, or in 40 microseconds. This is based on the practical assumption that a change in the smallest bit should produce an entirely new bit setting. The maximum slope $2\pi f_{max}$ of the sine wave of maximum frequency for 10-bit conversion must equal the maximum allowed change during conversion, so that

$$f_{max} = \frac{2^{-10}/40(10^{-6})}{2\pi} = 3.9 \text{ cycles/second.}$$

C. Resolution and Accuracy

Resolution is defined as the precision with which the analog-to-

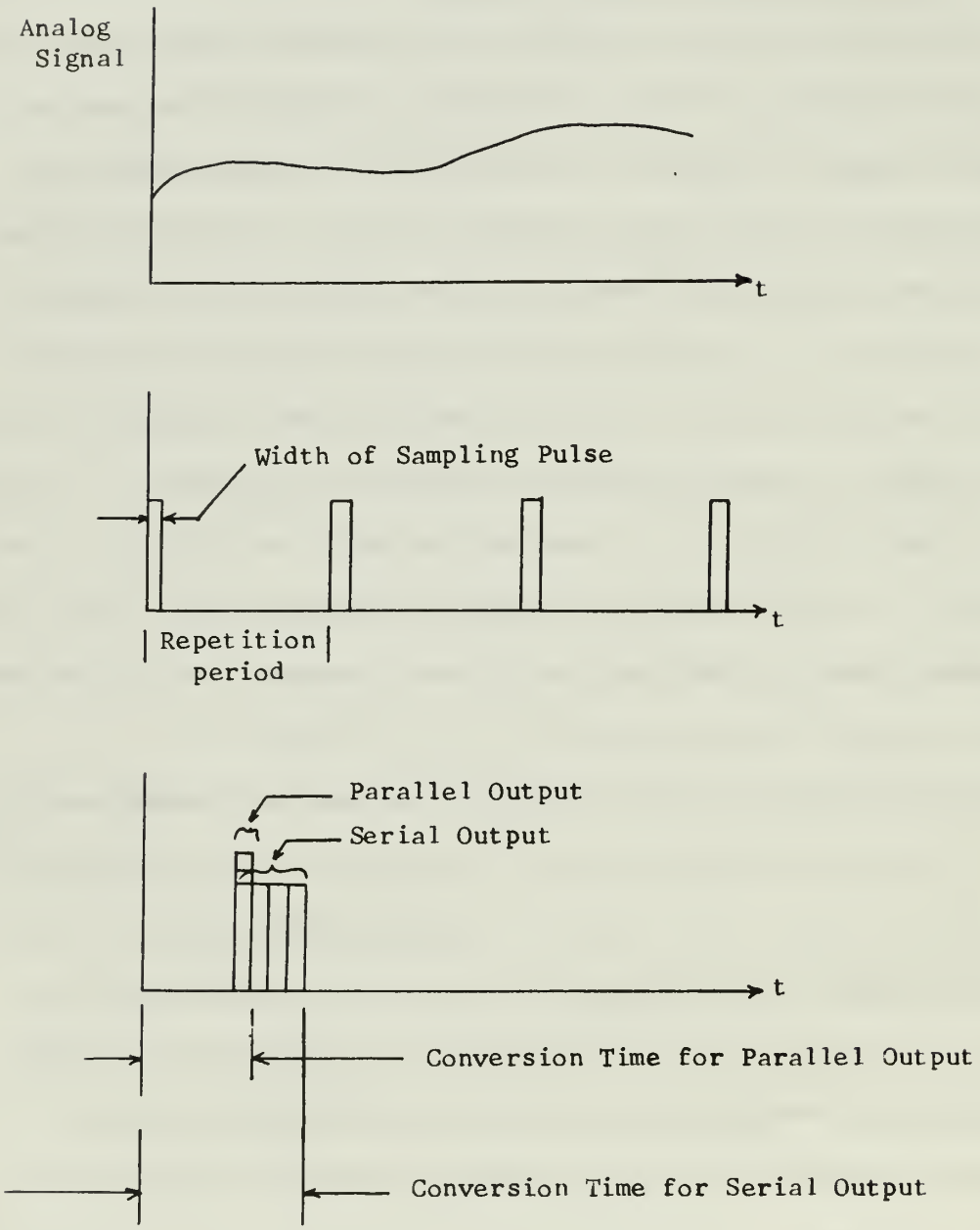


Figure 2.1. Analog-to-Digital Conversion Time

digital conversion can be accomplished. It is usually given by the least significant bit. Perhaps, this can best be seen by drawing an analogy with a radar system. How close can two targets be located and still be distinguished as two targets by an observer? For a binary coded output the precision with which a signal can be encoded is 2^{-n}, where n = number of bits. Thus 2^{10} = 1024 which gives a resolution of approximately 0.1%.

Usually the basic accuracy is taken to be the same as the resolution of the converter.

D. Possible Ambiguities in Output Data

The ambiguity problem arises because we want to be certain that as the analog input changes in a continuous way from one sampled level to another that the coded digital output changes by only one bit. If there is more than one bit change between levels there can be a marginal region where an erroneous digital output reading is obtained. Essentially this is a problem of non-ideal switching. This is shown in figure 2.2. In figure 2.2 it is shown that there exists a marginal region between two levels where switching may or may not occur. If several switches are required to switch simultaneously to determine one level from another, then ambiguities in the value of the digits, representing the analog value, can occur. This concept depends upon the particular code and is best illustrated by example 2.2.

Example 2.2: Given: Figure 2.3. The problem of ambiguity is best shown in the interval between levels 3 and 4. In level 3 the binary value of the signal = 0011 = decimal 3. In level 4 the binary code is 0100. There are three switchings which must occur in going from level 3 to level 4. Due to non-ideal switching properties of physical components the binary output in the overlap region can have any of the values given below:

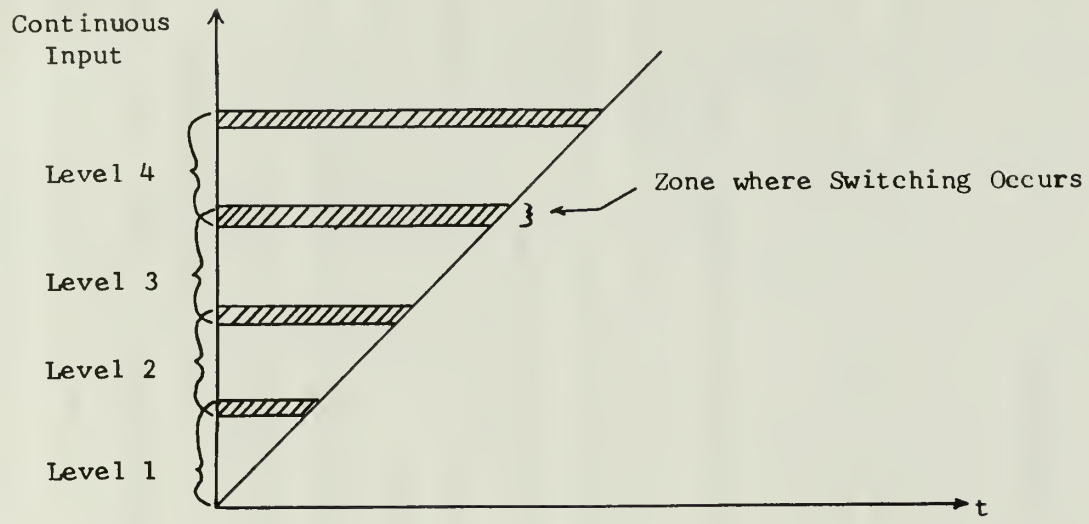


Figure 2.2. Non-ideal Switching Levels

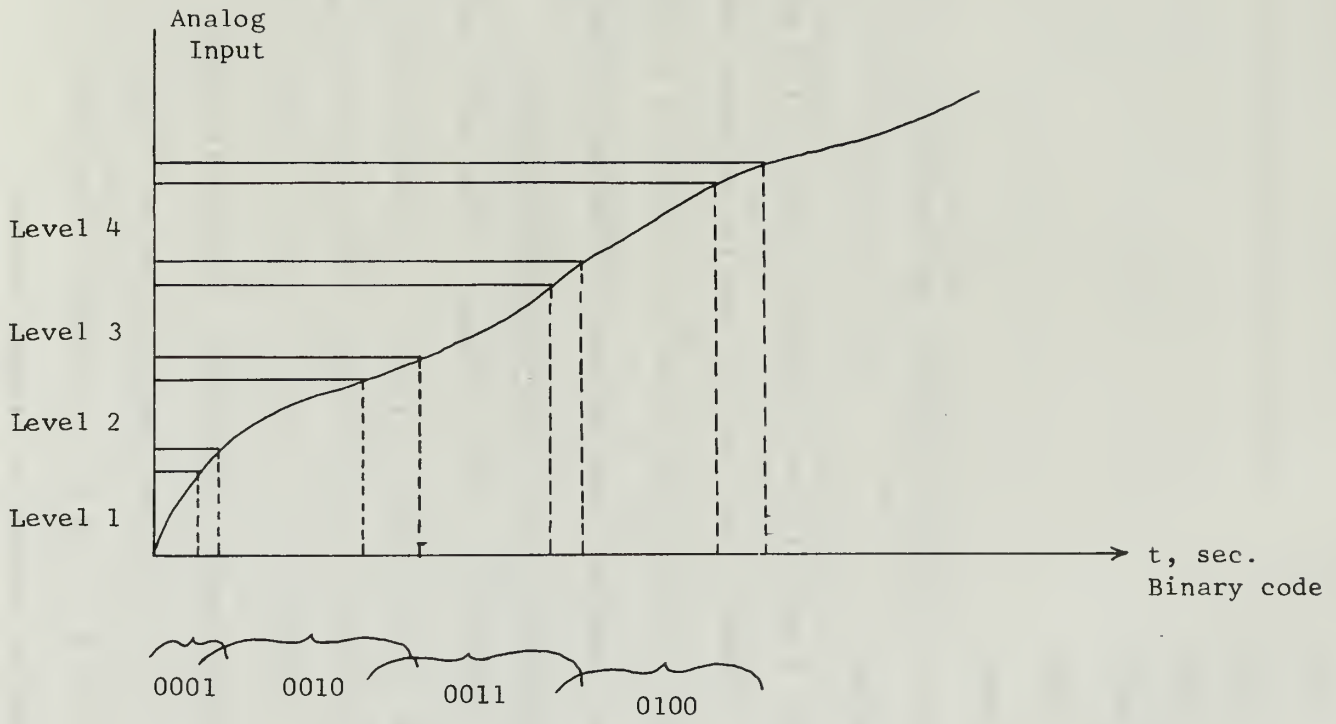


Figure 2.3. Quantization of Continuous Signal

0100 correct value

or 0111

0110

0101

0022

0010

0001

0000

There are several solutions that have been devised to take care of the ambiguity problem:

(a) Using a unit distance code (Gray code) [6] in which each successive level differs by only one bit from the adjacent level. Unfortunately this type of coded output cannot be expected to be compatible with normal digital computer codes and code conversion is required.

E. Temporary Storage or Data Holding Characteristics

Sample-hold circuits are analog storage devices which permit readout and/or storage of the value, $f(t_1)$, of a variable voltage f(t) at a specified sampling instant t_1. [7] In the conversion of analog quantities to digital form, it is often necessary to insure that the analog input quantity being sampled remains essentially constant throughout the conversion interval. [4] Either the sampling conversion time is short enough to insure this fact, or it is necessary to maintain the input quantity in a temporary storage or clamping device.

Additionally, in the conversion process from digital to analog, it is also necessary to maintain the digital number until the conversion is complete. Digital registers in this case will serve the function of data holding.

F. Adaptability for Time Multiplexing

Klein et.al. have given a general definition for time multiplexing. "Multiplexing - the time sharing of a single transmission channel by several independent information sources - allows a reduction in the amount of equipment used for the transmission and processing of this information." [8] It is possible to multiplex in two distinctly separate manners. These are:

(a) Fixed time intervals.

(b) On demand by information rate.

Fixed Time Multiplexing: The switches, as shown in figure 2.4, which determine the input information channel, are cycled at a constant frequency (clock device). At the clock frequency the following states result: 00, 01, 10, 11, and then repetition starts again.

Demand Multiplexing: In this method, when an input signal is not changing it is unnecessary to change the encoding because everything is progressing in order. However, when a signal starts changing, it is desired to override the clock controlling the multiplexer until output signal is encoded within the desired limits. This is accomplished, as shown in figure 2.5, by the use of a rate computer to establish when the rate of a signal exceeds some preset rate. At this time the central computer over-rides the clock in controlling the matrix to hold the desired channel on the output. [8]

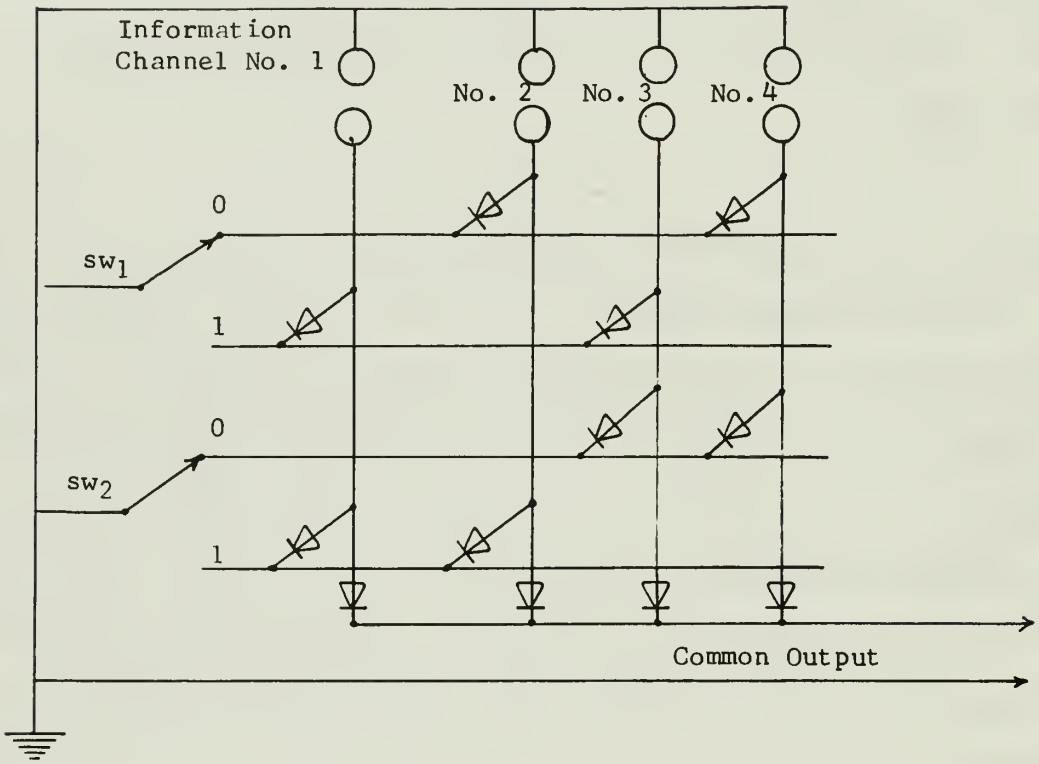


Figure 2.4. Fixed Time Multiplexing

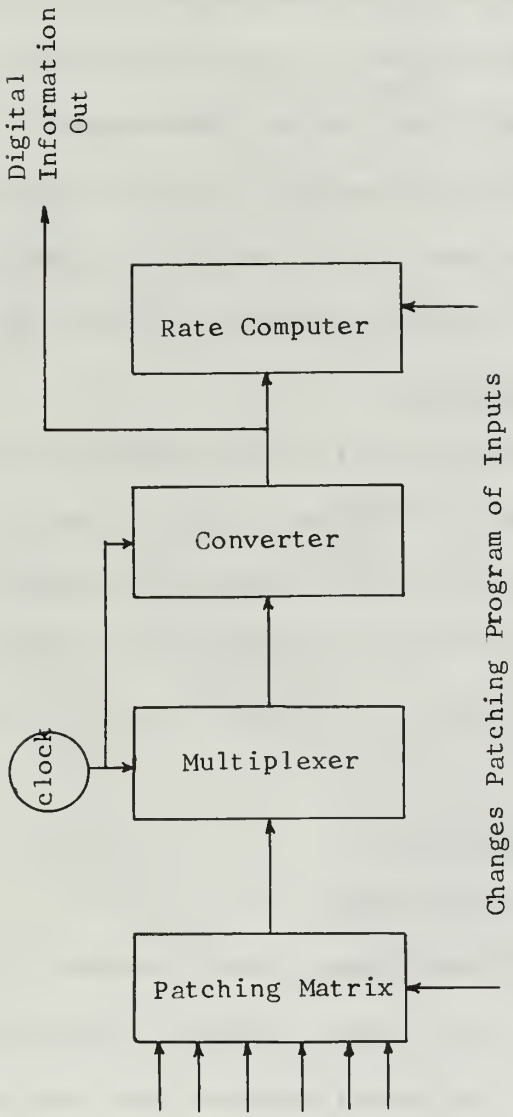


Figure 2.5. Demand Multiplexing

3. Electromechanical Converters.

Electromechanical converters utilize transducers which will transform physical motion into an equivalent electrical signal. They are generally of two basic types: continuous or quantized. [9] The continuous type implies that the motion of a shaft, whether it be angular or translational, may be represented by an analogous continuous electrical voltage. On the other hand, it may be desired to measure shaft motion by coupling a coding device on the shaft itself which, when sampled, yields the position of the shaft. A device of this nature is shown in figure 3.1. In this case the quantizing transducer is the coding disc itself. A diagram depicting the two general types of conversion is shown in figure 3.2.

A. Continuous Transducer

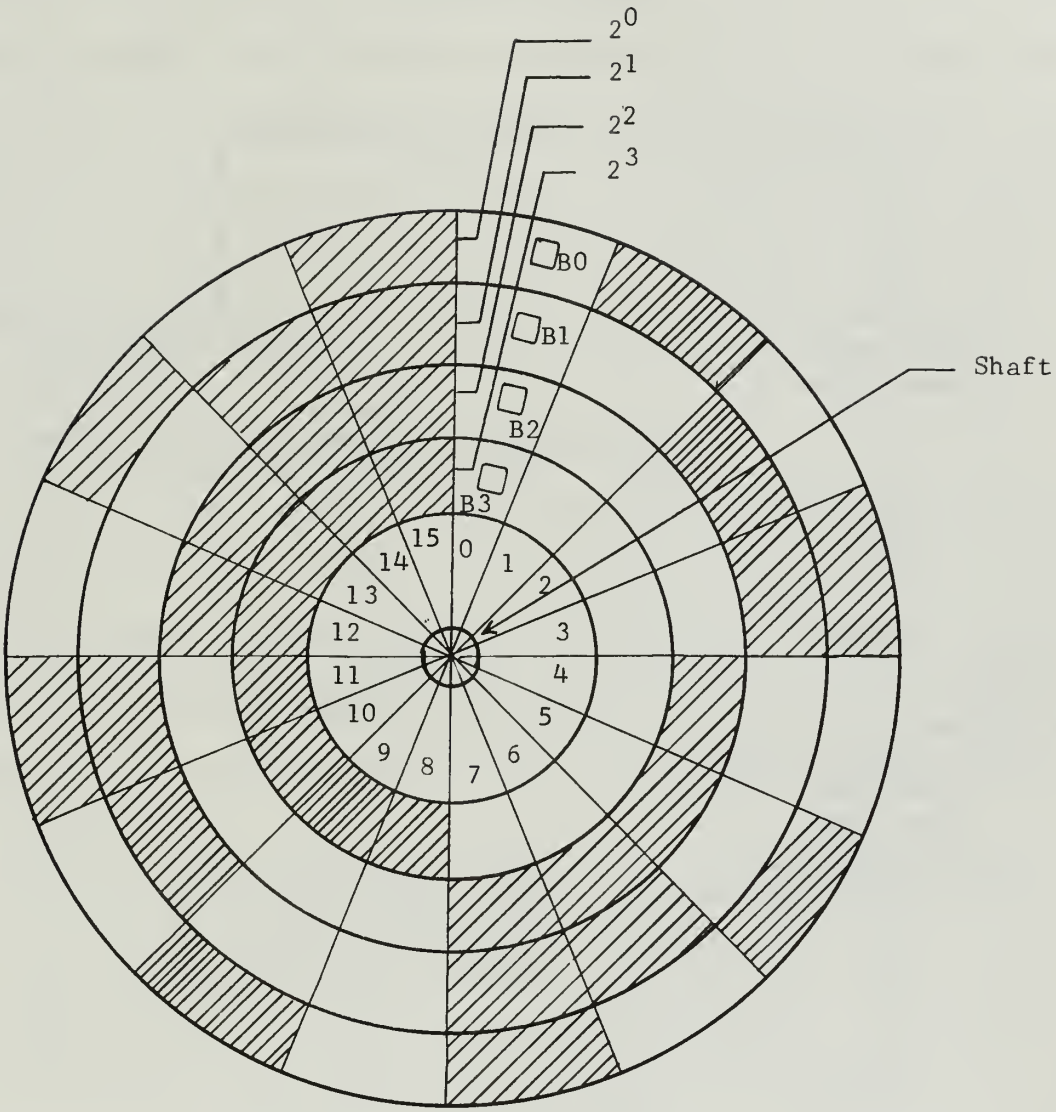
A continuous transducer requires the transformation of shaft position or rotation to an analogous electrical signal. Some of the continuous transducers employed today are potentiometers, synchros, and resolvers. The output here is an electrical signal that must now be sampled and converted to its digital representation by an electronic converter which is discussed in Section 4.

B. Quantized Transducers

I. Coded Pattern Devices

This technique utilizes a shaft encoder to give a binary digital measurement of a shaft angle position. This measurement may be used as a direct input to a digital computer from sensors which measure, for example, inertial platform orientation or antenna angles. [10]

The shaft encoder usually provides a high degree of stable accuracy in the conversion process from angle to digital representation. This is mainly due to the fact that the accuracy is built into the encoder by mechanical means and is not subject to drift or calibration. [10] Devices



Legend: B0 - B3 Reading Brushes. The decimal number denotes the value of that particular channel.

Figure 3.1. Coding Disc

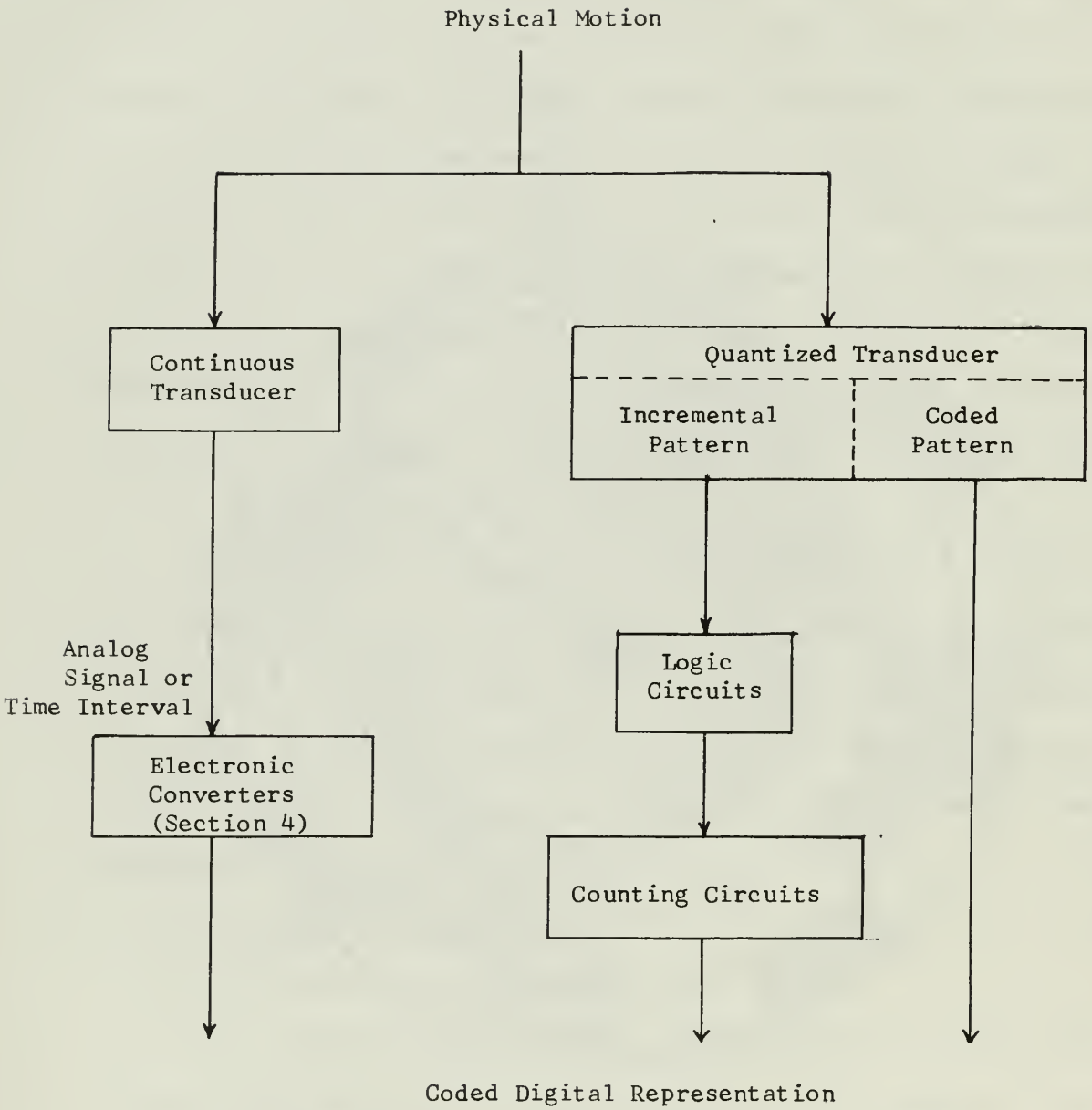


Figure 3.2. Methods for Position Coding

having resolution of one part in 2^{19} are commercially available. [11]

Since this type of encoder often uses a binary coding scheme, the ambiguity problem is of great importance. For the binary coded disc there are several techniques available to handle ambiguity. These include the V-brush method and V-brush method with self switching. Other techniques are to change the shaft encoding disc to a unit distance code. Although this technique eliminates ambiguities the problems of accuracy and code conversion still remain. The above techniques are discussed in detail in this section. Other types of coding schemes available are listed in Appendix A.

a. V-Brush Method for Binary Coding

The V-brush technique was developed by several manufacturers to handle the problem of ambiguity which may arise from non-ideal switching of the pickup devices from the binary coded disc as depicted in figure 3.1. The sampling of the coded disc may be done in one of two methods: (1) parallel, (2) serial [10]. The parallel implementation is shown in figure 3.3.

The theory of operation here is such that the brush to be sensed in track N_n depends on the brush sensed in track N_{n-1}. The logic required for readout follows: (1) Read the least significant track. (2) If the value of the least significant track = 1, select the lagging brush in the next track. (3) If the value of the least significant track = 0, select the leading brush in the next track. This logic process continues until all tracks have been read. The Boolean equation required for this implementation is:

$$N_n = \overline{N_{n-1}} \cdot B_n^* + N_{n-1} \cdot B_n \qquad (3.1)$$

See Figure 3.3.

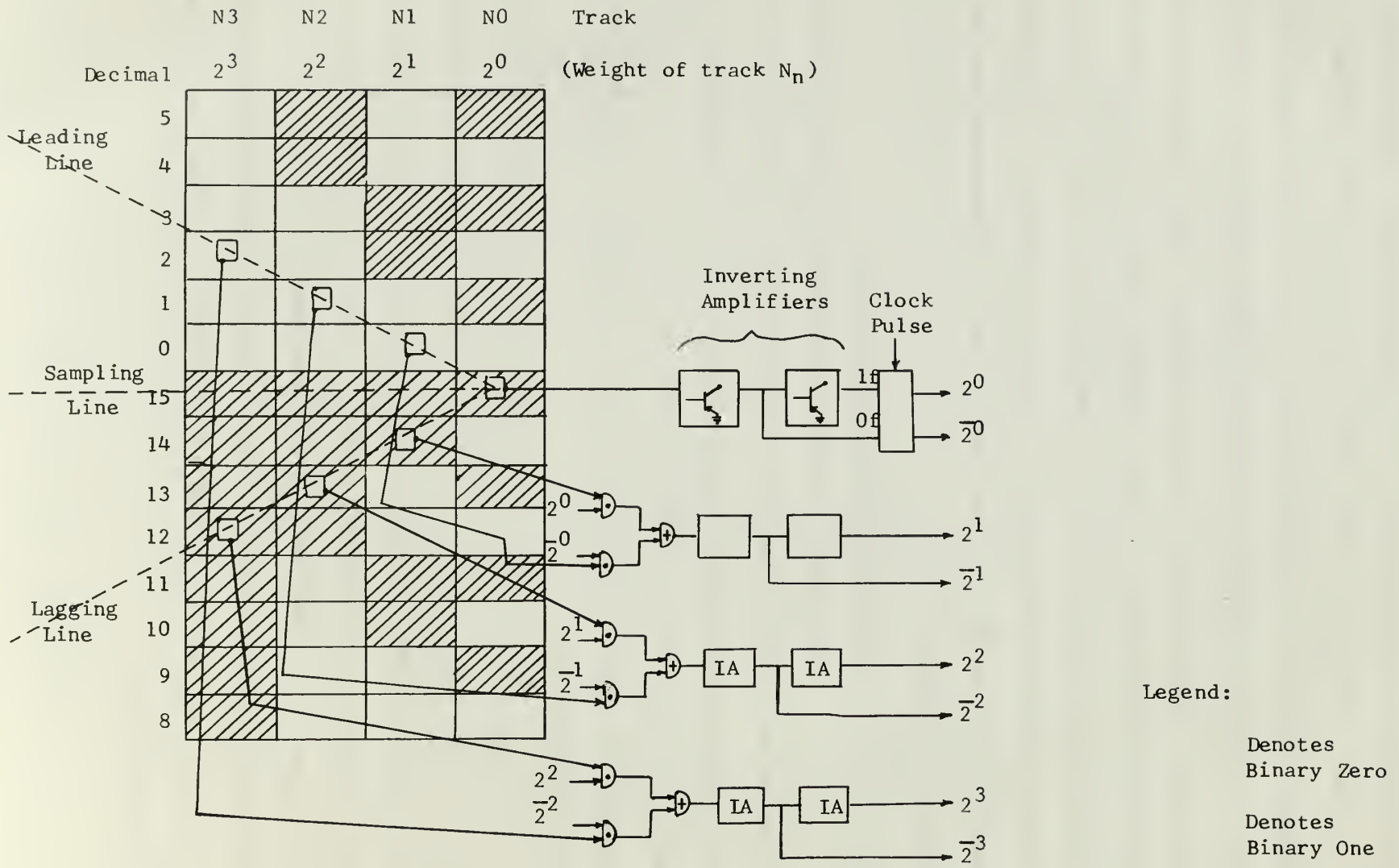


Figure 3.3. V-Brush Technique (Parallel Output)

where: N_n = value of n^{th} track.

N_{n-1} = value of n-1 track.

$\overline{N_{n-1}}$ = complement of the n-1 track.

B_n = lagging contact for the n^{th} track.

B_n^* = leading contact for the n^{th} track.

The following two examples illustrate the logical selection of the brushes to be senses.

Example 3.1: Given figure 3.4, find the binary code on the sampling line.

Solution: Track $N_0 = 0$, therefore track N_1 must sample the brush on the leading line $N_1 = 1$, $N = 1$ then track N_2 must sample brush on lagging line $N_2 = 1$, then N_3 samples brush on lagging line $N_3 = 1$. Binary representation obtained from this sampling process = 1110 = decimal 14.

Example 3.2: Given figure 3.5, find the binary code on the sampling line.

Solution: Track $N_0 = 1$, therefore sense lagging brush in track N_1, $N_1 = 0$ therefore sense leading brush in track N_2, $N_2 = 1$ therefore sense lagging brush in track N_3, $N_3 = 1$. Binary code = 1101 = decimal 13.

It is possible to time share the logic circuitry for several code wheels and brushes. This is accomplished by connecting a common lead to all encoders. An addressing signal from the computer denotes which encoder is to be sampled. The sampled output from the shaft encoder is available to the computer in parallel form on demand.

The serial encoding V-brush technique is used with a serial input computer. In this technique pulses generated by the computer are required to energize "and" gates for successive tracks starting with the

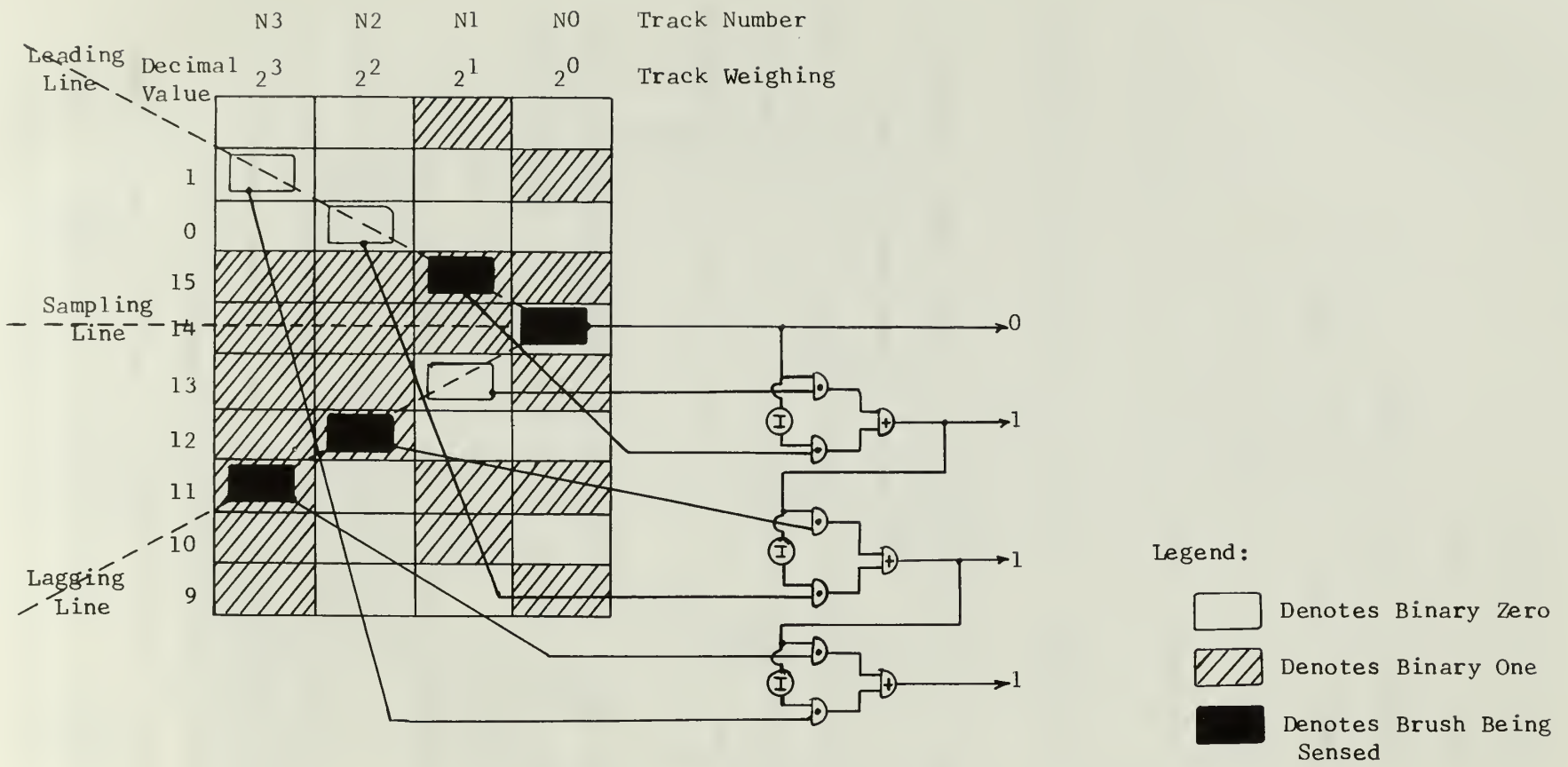


Figure 3.4 for Example 3.1

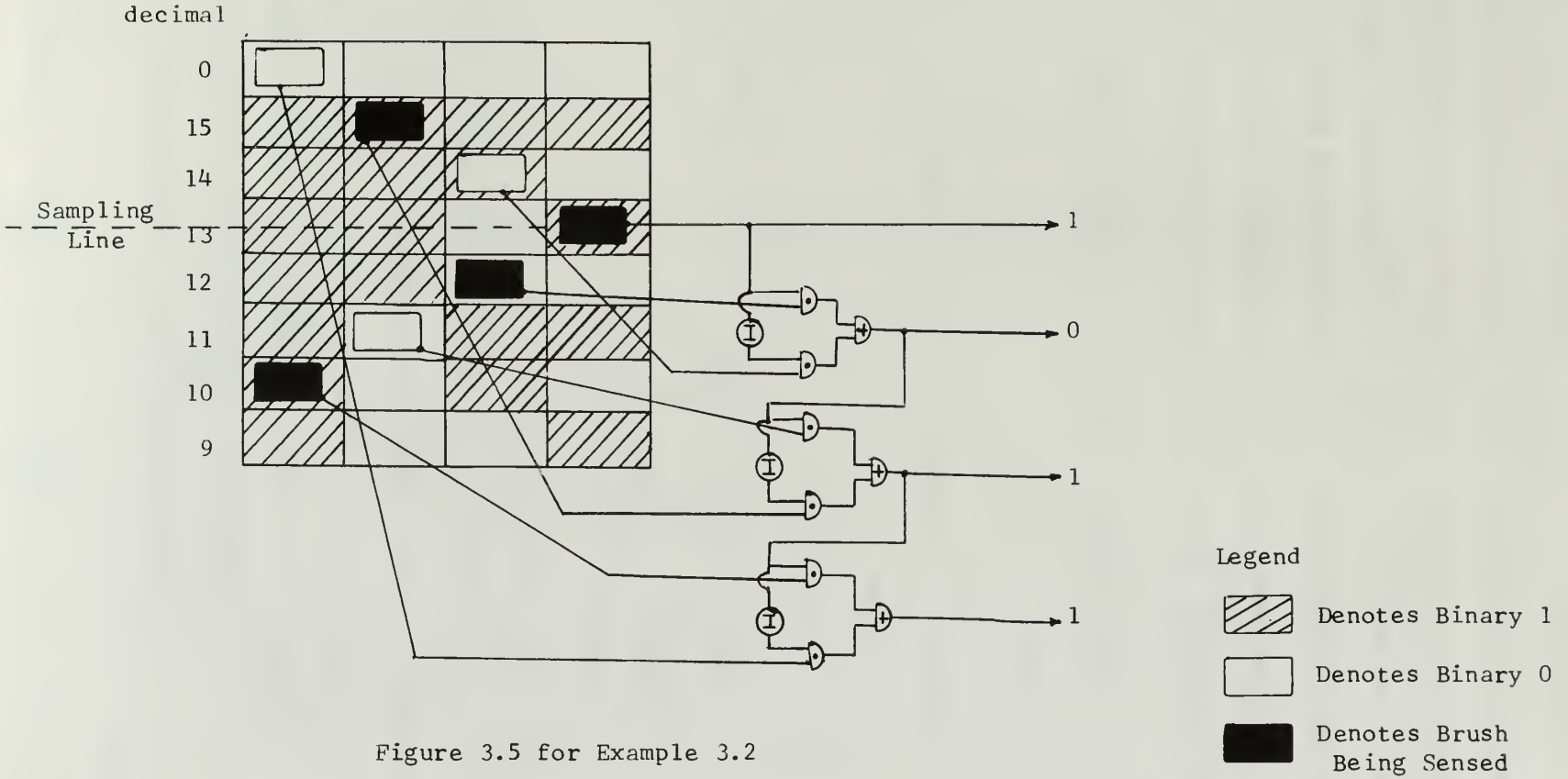


Figure 3.5 for Example 3.2

least significant track. The least significant track (N_0) is energized by a common lead between the computer and encoders used for addressing the code wheel to be sampled. The value of the least significant track is stored in the set-reset flip-flop and the succeeding "and" gates are energized one at a time, until all tracks have been sensed.

The logic implementation of this technique is given in figure 3.6. The Boolean equations for the input signal to a set-reset flip-flop are: [10]

$$1f = P_0B_0 + P_1B_1^{*}F + P_1B_1\overline{F} + \cdots + P_nB_nF + P_nB_n^{*}\overline{F} \qquad (3.2)$$

$$0f = \overline{1f} \qquad (3.3)$$

where P signals are generated by central computer.

B_n = lagging contact for the n^{th} track.

B_n^{*} = leading contact for the n^{th} track.

F = (N_{n-1}) track for the parallel case, in this case the value of the flip-flop.

$\overline{F}$ = ($\overline{N_{n-1}}$) complement of F.

1F = input to set-reset flip-flop.

$0f = \overline{1f}$ = complement of 1f.

Since this technique is being used for an input to a serial computer, the samples are still available on demand.

The advantages of the two techniques discussed are: (1) Samples are available on demand to the digital computer. (2) Time sharing of the external logic circuitry can be accomplished by placing isolation diodes on the coding disc and using a common lead to address and select the encoder. [10]

The loading effect of the code wheel encoder is listed in Table 3.1.

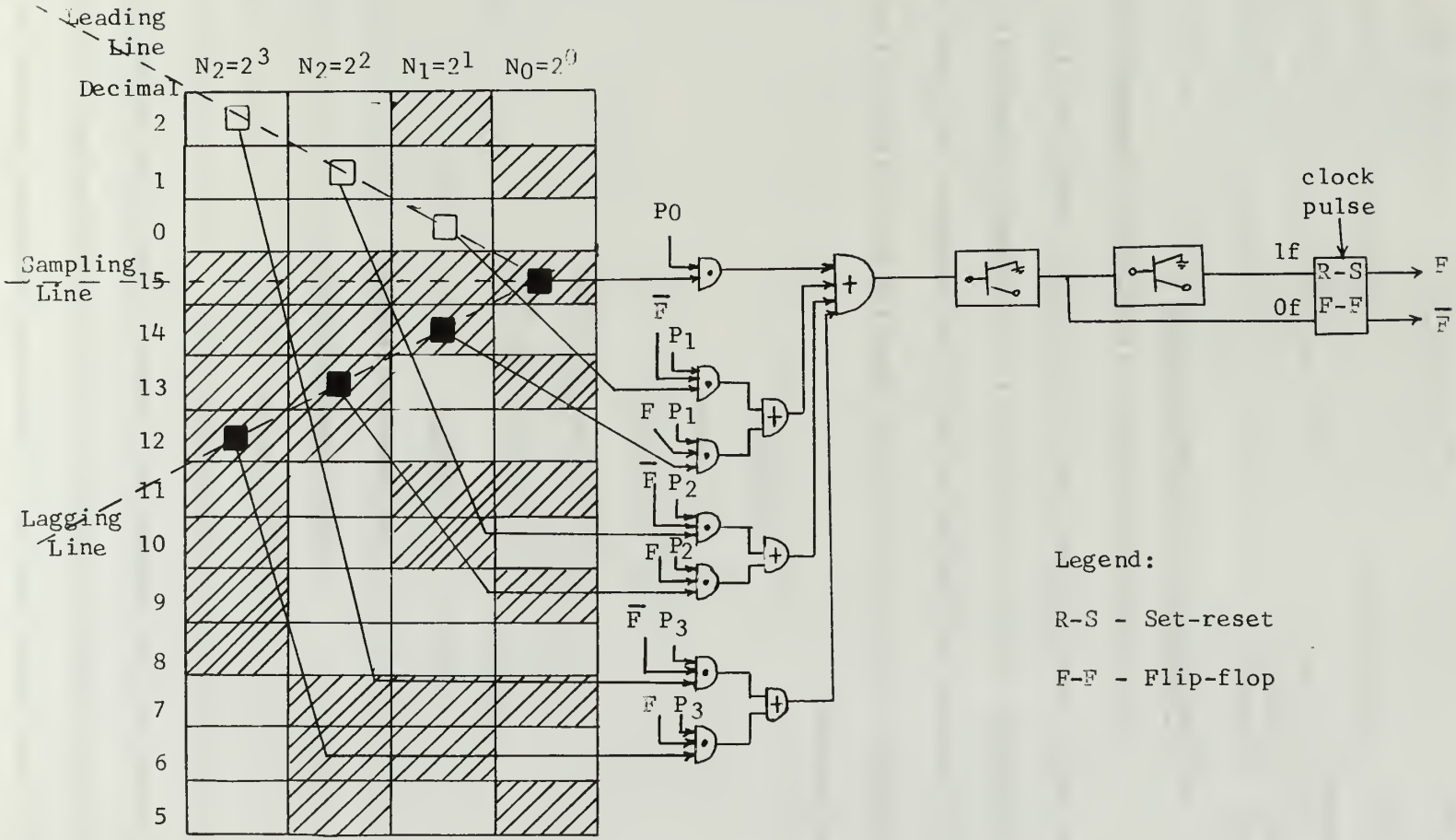


Figure 3.6. V-Brush Technique (Serial Output)

TABLE 3.1

	8 bit coding	13 bit coding
Length	1.062 in.	1.828 in.
Weight	1.66 oz.	3.08 oz.
Diameter	1.062 in. $\pm$ .005	1.062 in. $\pm$ .005
Moment of inertia	.01 oz. in.^{2}	.02 oz. in.^{2}

b. V-Brushes with Self-Switching

In the preceding section the V-brush technique was discussed as one of the possible ways of encoding a shaft position. The main disadvantage of such a technique is the amount of external circuitry required to achieve the coding process. For example, the parallel and serial implementation (11 bit coding) requires the following functions to be implemented:

Parallel

20 "or" gates

10 "and" gates

22 Inverting Amplifiers

1 set-reset flip-flop

Serial

1 set-reset flip-flop

2 Inverting Amplifiers

21 "or" gates

1 "and" gate

The number of basiccomponents; diodes, biasing resistors, transistors, and power supplies, depends on the logic scheme used (i.e. NAND, NOR, AOI, etc). The V-brush with self switching technique reduces the amount

of external circuitry required. The logic operations, in this technique, are performed on the coded disc. This is accomplished by the addition of two more brushes or pickup devices to each track and the coded disc is constructed in a different manner from that discussed previously. Both the zero and one portions of each track are constructed of conducting material but insulated from each other and tracks are also insulated from each other. The operation of this technique is shown in figure 3.7. For the purpose of illustration, assume that brush B_0 is ideal and can switch instantaneously. [9] Then the logic is such that:

$$(1)\ \text{If}\ \ B_0 = \begin{cases} 0 \text{ select } B_1^* \text{ in track } N_1 \\ 1 \text{ select } B_1 \text{ in track } N_1 \end{cases}$$

$$(2)\ \text{if}\ \ B_1 = \begin{cases} 0 \text{ select } B_2^* \text{ in track } N_2 \\ 1 \text{ select } B_2 \text{ in track } N_2 \end{cases}$$

$$\vdots$$

$$(n)\ \text{If}\ B_{n-1} = \begin{cases} 0 \text{ select } B_n^* \text{ in track } N_n \\ 1 \text{ select } B_n \text{ in track } N_n \end{cases}$$

where n = 0, 1, 2, 3,.... the number of encoding bits.

Unfortunately, reading devices such as brushes are not ideal and a modified approach must be used. This approach is to modify the N_0 track and sense if B_0 is on a "one" or "zero." Any bistable decision device such as a flip-flop can accomplish this purpose. [12] Using the following procedure: if the electrical circuit, as shown between brush B_0 and B_0^* in figure 3.8, is completed, output = 1, select lagging brush B_1 in track N_1. If open circuit on track N_0 then flip-flop output = 0, select leading brush B_1^* in track N_1. In this technique only two diodes

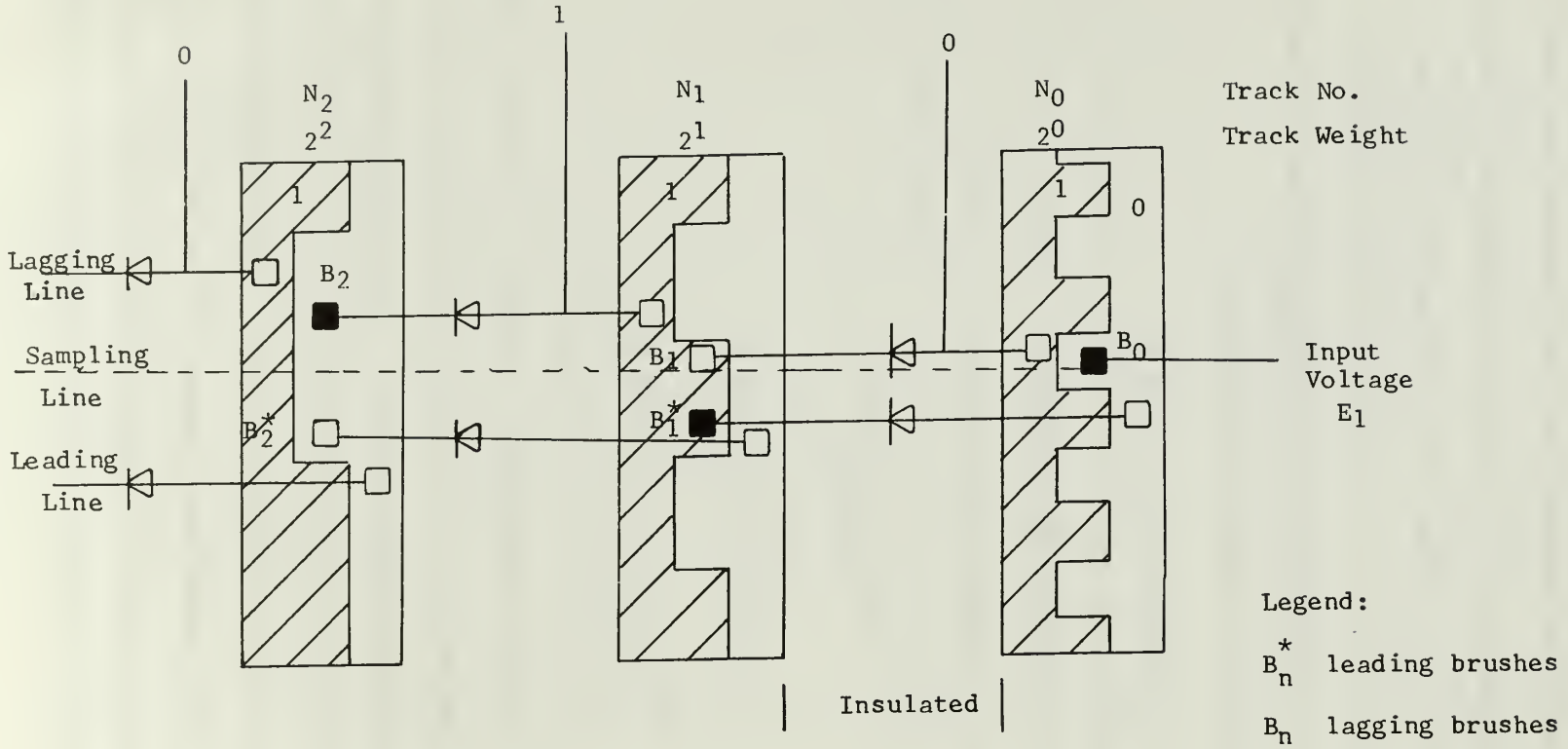


Figure 3.7. V-Brush Technique with Self Switching

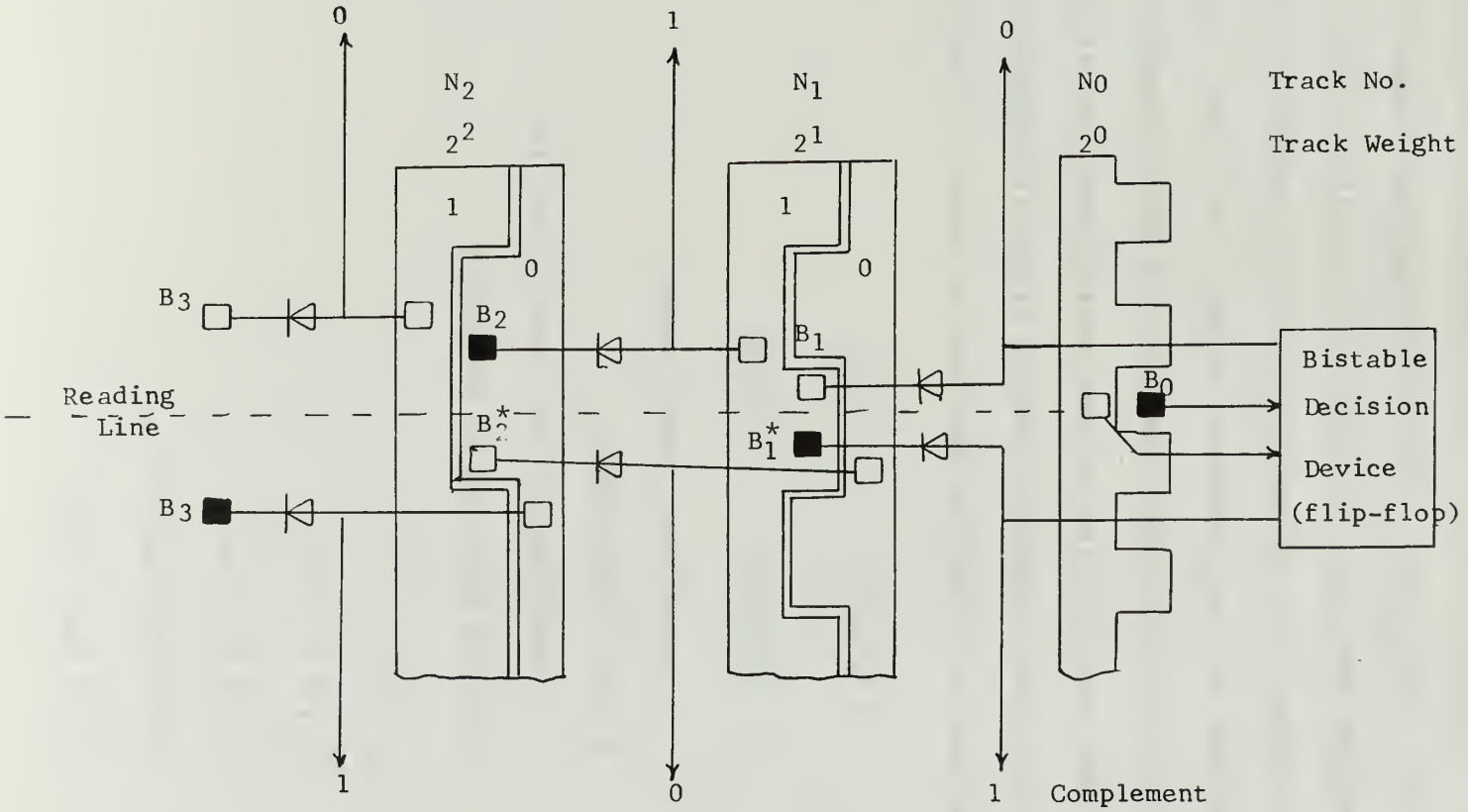


Figure 3.8. Practical V-Brush Technique with Self Switching

per track (bit) are required and the only external circuitry required is the bistable decision element as shown in figure 3.8.

C. Unit Distance Encoder

The unit distance or Gray [6] code changes only one bit between consecutive levels. Since only a single brush switches between code positions the maximum error that can occur in the position of the shaft is one level of coding. [4] The Gray code is not a weighted code (that is, bit position does not carry numerical weight). This code in general is not compatible with most digital computers and code conversion must be performed. Gray code for first sixteen decimal positions is given in Table 3.2. Other unit distance codes are listed in Appendix A. The Boolean equations for converting Gray code to binary follows: [13]

$$C = C_n C_{n-1} C_{n-2} \cdots C_2 C_1 C_0 \tag{3.4}$$

$$G = G_n G_{n-1} G_{n-2} \cdots G_2 G_1 G_0 \tag{3.5}$$

where C = conventional binary number.

G = Gray code number.

C_n = conventional binary term in position n.

G_n = Gray code term in position n.

$$C_n = G_n \tag{3.6}$$

$$C_{n-1} = G_n + G_{n-1}$$

$$C_{n-1} = C_n + G_{n-1} \tag{3.7}$$

$$C_{n-2} = G_n + G_{n-1} + G_{n-2}$$

$$C_{n-2} = C_{n-1} + G_{n-2} \tag{3.8}$$

.
.
.

TABLE 3.2

Gray Code - 4 Bits

Decimal	Gray Code
0	0000
1	0001
2	0011
3	0010
4	0110
5	0111
6	0101
7	0100
8	1100
9	1101
10	1111
11	1110
12	1010
13	1011
14	1001
15	1000

$$C_2 = C_3 + G_2 \tag{3.9}$$

$$C_1 = C_2 + G_1 \tag{3.10}$$

$$C_0 = C_1 + G_0 \tag{3.11}$$

General formula [13]

$$C_s = \sum_{t=s}^{n} G_t \tag{3.12}$$

Example 3.3: Gray code = 1001 = decimal 14.

Solution: $n = 3$, $G_3 = 1$, $G_2 = 0$, $G_1 = 0$, $G_0 = 1$.

$$C_3 = G_3 = 1$$

$$C_2 = G_3 + G_2 = 1 + 0 = 1$$

$$C_1 = C_2 + G_1 = 1 + 0 = 1$$

$$C_0 = C_1 + G_0 = 1 + 1 = 0$$

Binary number = $C_3C_2C_1C_0$= 1110.

Checking the solution:

$$1 \cdot 2^3 + 1 \cdot 2^2 + 1 \cdot 2^1 + 0 \cdot 2^0 = 8 + 4 + 2 = \text{decimal } 14.$$

Implementation of code conversion (Gray to binary) operations is shown in figure 3.9. The disadvantage of using a Gray encoding wheel is the amount of external logic circuitry. For 11 bit coding the number of logic operations that must be implemented are: 22 inverters, 10 "and" gates, and 20 "or" gates. The number of basic elements such as diodes, biasing resistors, transistors, and power supplies still depend on logic scheme used (i.e. NAND, NOR, AOI, etc.). The advantages of this type of encoding are: samples available on "demand" and the external logic circuitry can be time shared between encoders in the same manner as that for the parallel V-scan implementation technique.

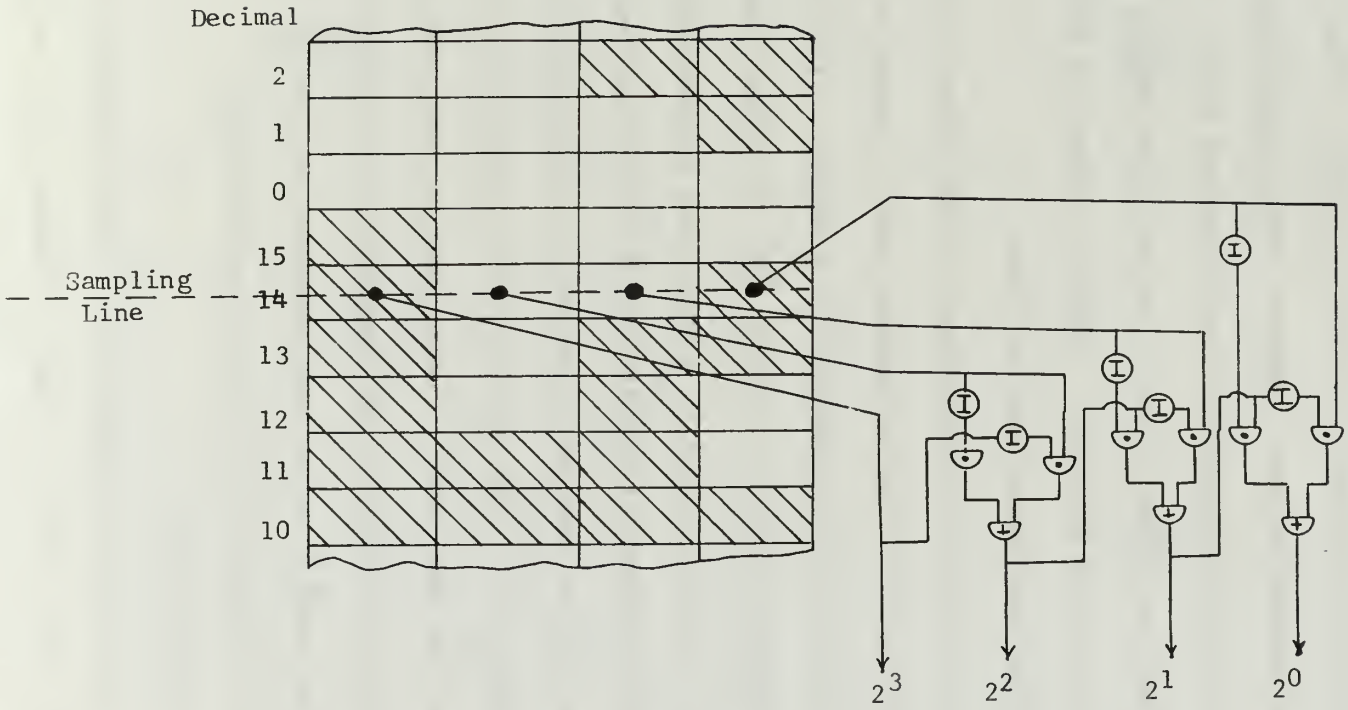


Figure 3.9. Gray Code Conversion

II. Incremental Pattern Devices

Incremental pattern devices are one of the two general types of quantized transducers. According to Susskind [9], "the name implies that a signal is developed for each increment of motion and since the increment signals are indistinguishable, it is only known that position has changed by one increment when a signal is received." With this in mind there are two problems that must be solved. These are: the coding disc must be mounted in such a fashion that clockwise and counterclockwise motion can be distinguished and an up-down binary counter must be used to maintain an accumulation of pulses which denote shaft's position relative to the start position. These two items are discussed in detail in the following section on slotted discs.

There are two major disadvantages to this type of encoding scheme. The incremental pattern device measures only a change in position. These changes in position are accumulated in a counter. If a pulse should be lost all subsequent data is in error. [9] The other disadvantage is that the external circuitry cannot be time shared between encoding discs. This arises because incremental signals are derived from physical motion. Therefore the counter must be connected to the interpreting circuits, as shown in figure 3.11 at all times ready to receive an incoming signal. None-the-less the simplicity of these devices makes them practical. Also the accumulation of error can be compensated by periodically checking the output reading (such as after each complete revolution) to see if it is correct and to correct it if an error has occurred.

a. Slotted Disc

The simplest implementation of an incremental device is the slotted disc. Such a disc is shown in figure 3.10. In figure 3.10, it is shown that slits V_1 and V_2 are offset. The primary purpose of this

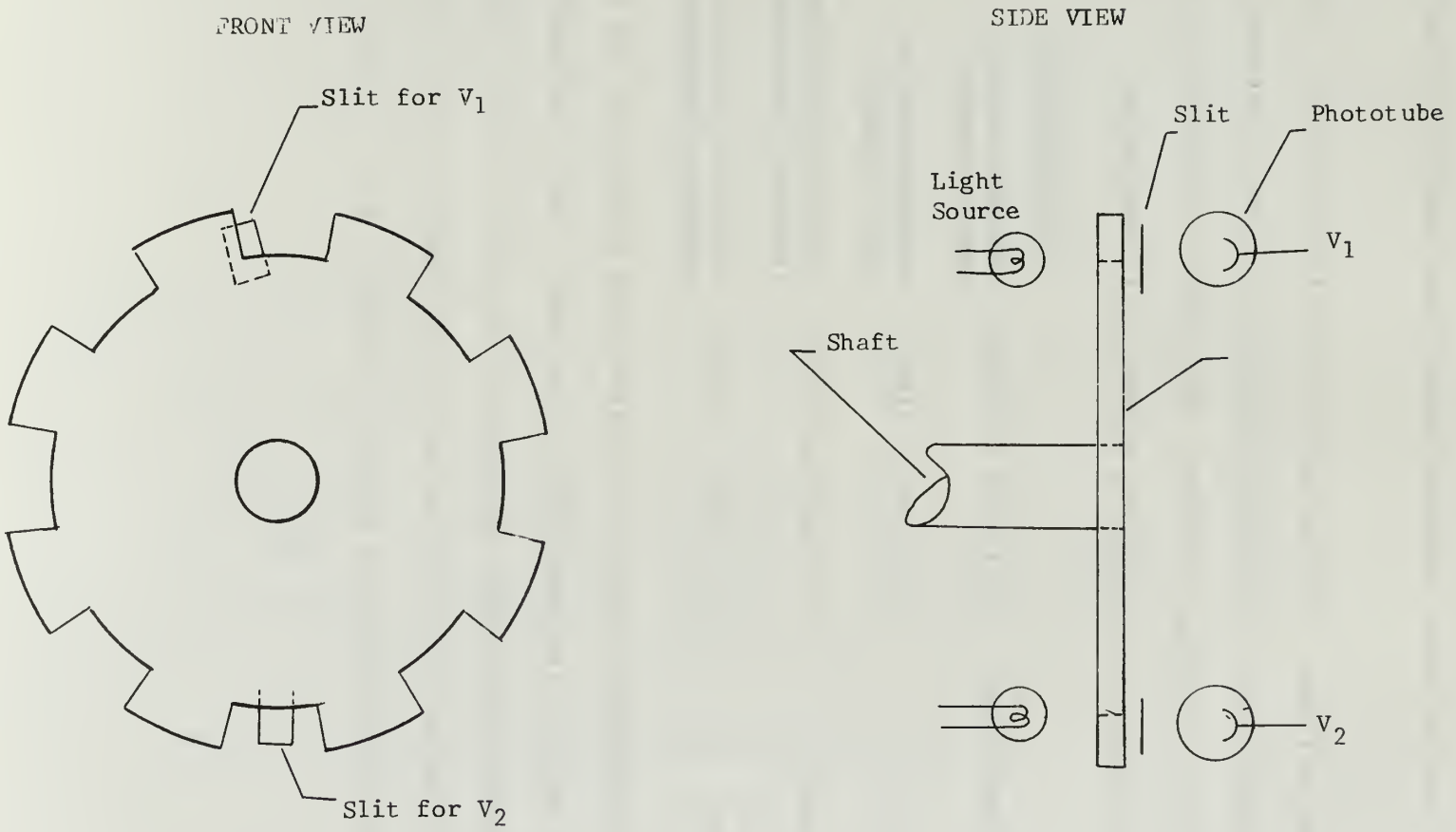


Figure 3.10. Slotted Disc

offset is to be able to implement logic circuits that interpret the direction of disc rotation. Although a light source is shown in figure 3.10 other detection means such as brush contacts, magnetic and capacitive coupling can be used.

It is shown in figure 3.10 that when V_2 is illuminated (from a light source) and V_1 goes from an illuminated position to a non-illuminated position the disc is rotating clockwise. Thus logic circuits can be implemented that determine the direction of motion as shown below:

		Interpretation
(1) V_2 (illuminated)	V_1 (light to dark)	clockwise motion (add increment)
(2) V_2 (dark)	V_1 (dark to light)	clockwise motion (add increment)
(3) V_2 (light)	V_1 (dark to light)	counterclockwise motion (subtract increment)
(4) V (dark)	V_1 (light to dark)	counterclockwise motion (subtract increment)

In this logic scheme a pulse is obtained every time one of the slits is illuminated and thus the resolution is one part in twice the number of slots. [9] Another scheme could utilize only one state of slit V_2 and thus the resolution would be only one part in the number of slots. [9] A simplified block diagram denoting the logic scheme is given in figure 3.11.

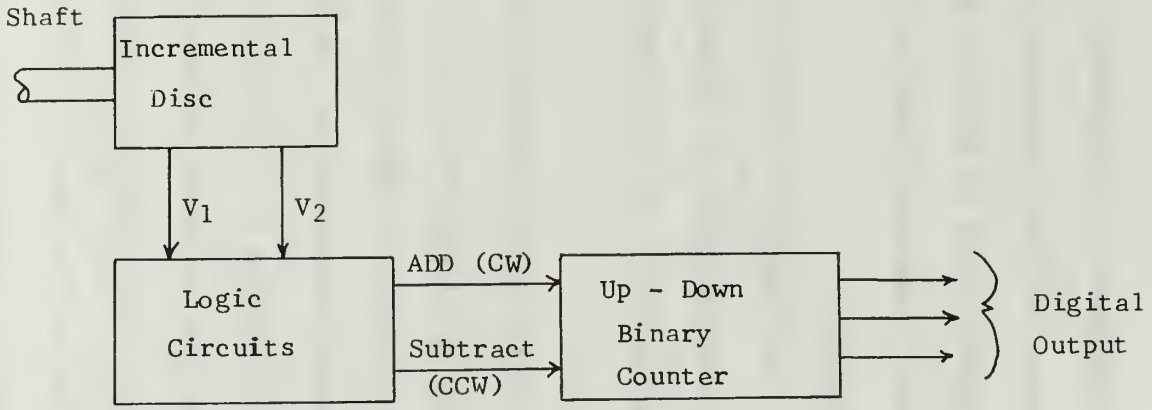


Figure 3.11. System Utilizing Slotted Disc Encoder

4. Electronic Converters

4.1. Analog-to-Digital. There are basically three methods for accomplishing analog-to-digital donversion utilizing all electronic ADC's. These methods are: [14]

(a) Simultaneous converters.

(b) Feedback encoding (voltage comparison).

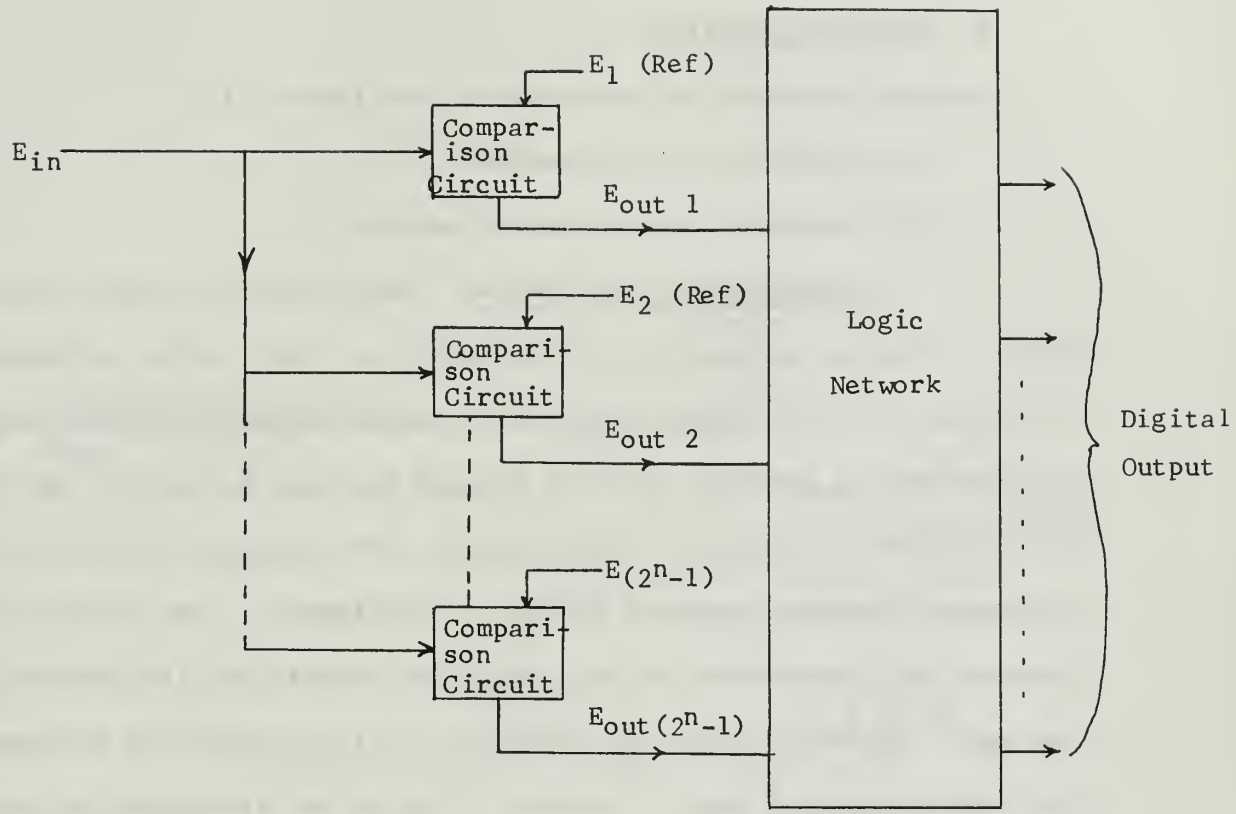
(c) Time base encoding.

These techniques are discussed in this section. It should be kept in mind that the input signals to these electronic converters can very well be the electrical representations of physical quantities such as those derived from continuous transducers (section 3).

A. Simultaneous Converters.

A technique which has been mentioned by the Digital Equipment Corp. [14] is the simultaneous converter which is characterized by its rapid (4-10 microseconds) conversion time. No other details are available, possibly for proprietary reasons.

The major drawback of this type of converter is that $2^n - 1$ comparators are required for coding a voltage into n bits. Additionally, logic circuitry is required to transform the outputs from the $2^n - 1$ comparators to the appropriate n-bit coded representation. A block diagram of this type of converter is shown in figure 4.1. From the legend given in the figure, it can be seen that the resolution of this type of converter is $E = \frac{Em}{2^n}$. The accuracy of the conversion technique is highly dependent on the accuracy and stability of the precise reference voltage supplies needed as well as the comparison circuits. If n = 10 and $\triangle E$ is of the order of 10 millivolts then $E_m = 10^{-3}\ 2^n = 10.24$ volts. Thus for 10 bit encoding, practical reference and comparison circuit performance (stability,



Legend: E_m = voltage range of the converter

n = number of binary digits in result

2^n = number of intervals into which E_m is subdivided

$$E = \frac{E_m}{2^n}$$

$$E_1 = E_m - \triangle E$$

$$E_2 = E_m - 2\triangle E$$

$$\vdots$$

$$E_j = E_m - j\triangle E$$

Figure 4.1. Parallel Encoding

hysteresis) lead to practical input voltage ratings. The largest disadvantage of this type of encoder seems to lie in the number of components required.

B. Feedback Encoding

Feedback encoders are generally of two types. [15]

(a) Continuous balance method.

(b) Successive approximation method.

I. Continuous balance method. The operation of this type of device is shown in figure 4.2. The output of a DAC, which is discussed in section 4.2, is compared with the incoming electrical signal and an error signal is produced which is clamped and used to control the direction in which the up-down counter moves. The accuracy of this type of converter (feedback encoder) depends on two factors. The accuracy (sensitivity and hysteresis) of the comparison circuit and the accuracy of the DAC. The sensitivity and hysteresis of the comparators in present day practice do not pose a problem. This can be illustrated by example 4.1. Comparators with a hysteresis of 5 millivolts are commercially available. [16]

Example 4.1: Given: 8 bit converter with an input voltage of $\pm$ 10 v. Find the effect of a 5 mv sensitivity band in the comparator.

Solution: Range of converter = 20 volts. Number of levels available for 8 bits = $2^8 - 1 = 255$. Therefore,

$$\frac{20 \text{ volts}}{255} = 78.5 \text{ mv/level} \gg 5 \text{ mv.}$$

The conclusion that can be derived from this computation is that the comparator's hysteresis has a small effect in the overall accuracy of the converter. The next point that must be investigated is the accuracy of the DAC. Rehn [17] has constructed a DAC which converts 11 bits to

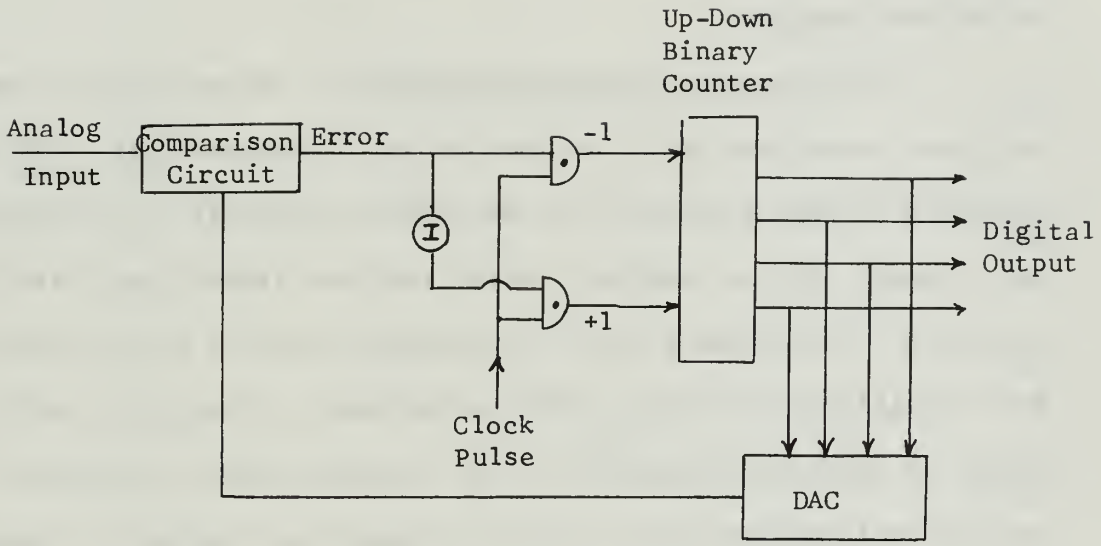


Figure 4.2. Continuous Balance Encoding

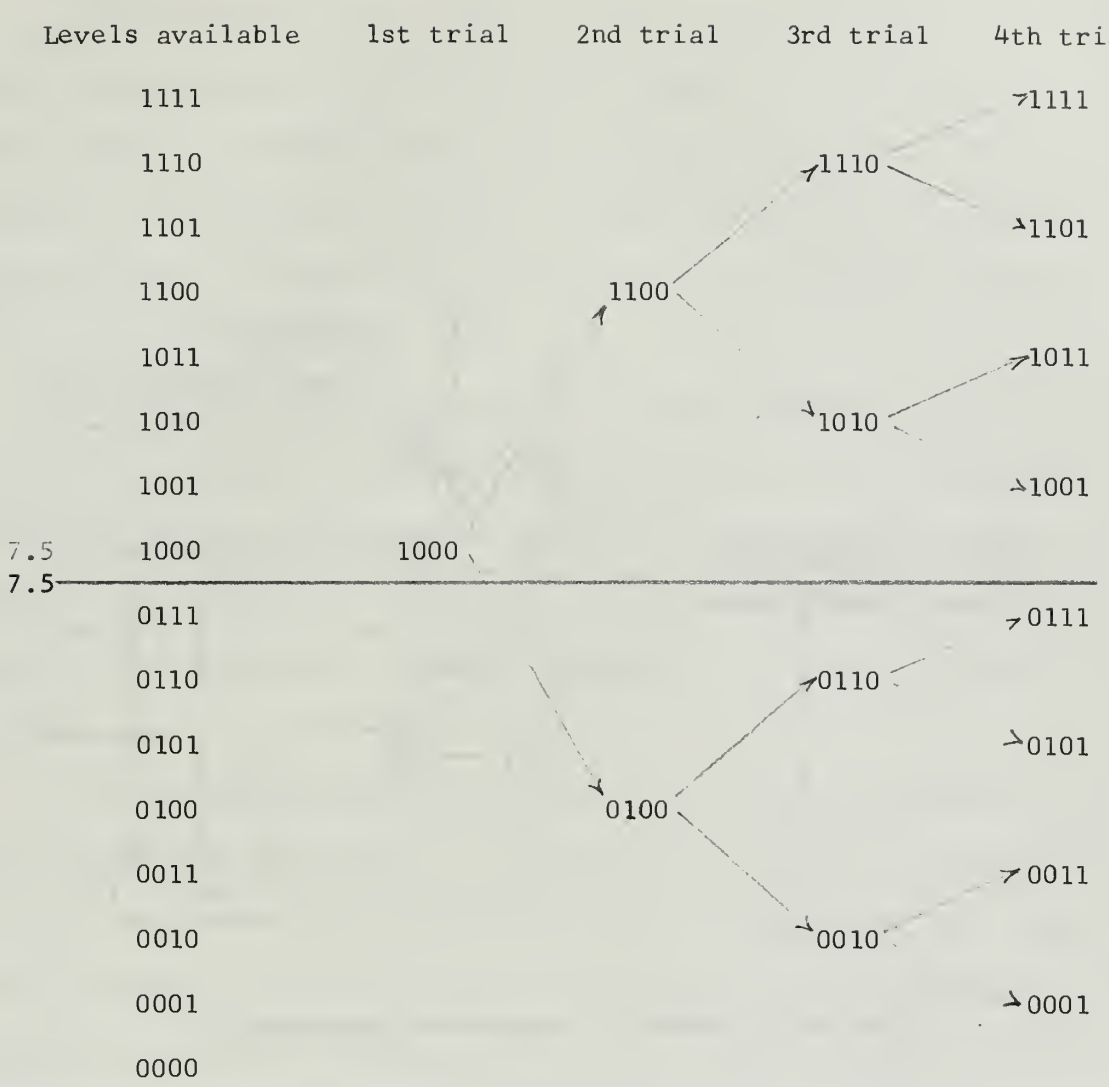
analog form in 8 microseconds with an accuracy of 0.05%. This was achieved by maintaining close tolerances on the critical resistors.

For coding a voltage in n-bits, the converter requires a maximum of $2^n - 1$ steps to cover its entire range [18] which with a 5 megacycle/second clock and a 10 bit conversion leads to a conversion time of approximately 200 microseconds. A slight modification of this technique leads to the successive approximation method of encoding a voltage as discussed in the next section.

II. Successive Approximation Method. The majority of commercially available electronic ADC's use this coding technique. [18] This mode of operation is such that prior to the sampling interval all flip-flops are set to zero. At the sampling instant the most significant flip-flop is turned on. The incoming signal is compared with the analog value of the most significant flip-flop. This establishes a situation in which half (upper or lower) the magnitude of the incoming signal is located. Based on this decision the logic circuitry proceeds to converge in successive trial steps on the value of the incoming signal. This action can best be illustrated in the following example.

Example 4.2: Given a converter with an input voltage range of 15 volts. An incoming signal is equal to 7.5 volts:

Solution:



Output digital number in this case = 0111.

From this example it can be seen that n steps are required to complete the conversion. This is in contrast to the continuous balance technique in which 2n-1 steps were required to cover the converter's range. The practical upper limit on the speed of conversion is 60,000 samples per second, [18] which is mainly due to the sequential nature of operation. It can be seen from figure 4.3 that this technique yields itself to time multiplexing by simply switching the input to the converter and transferring the bit setting to a storage register.

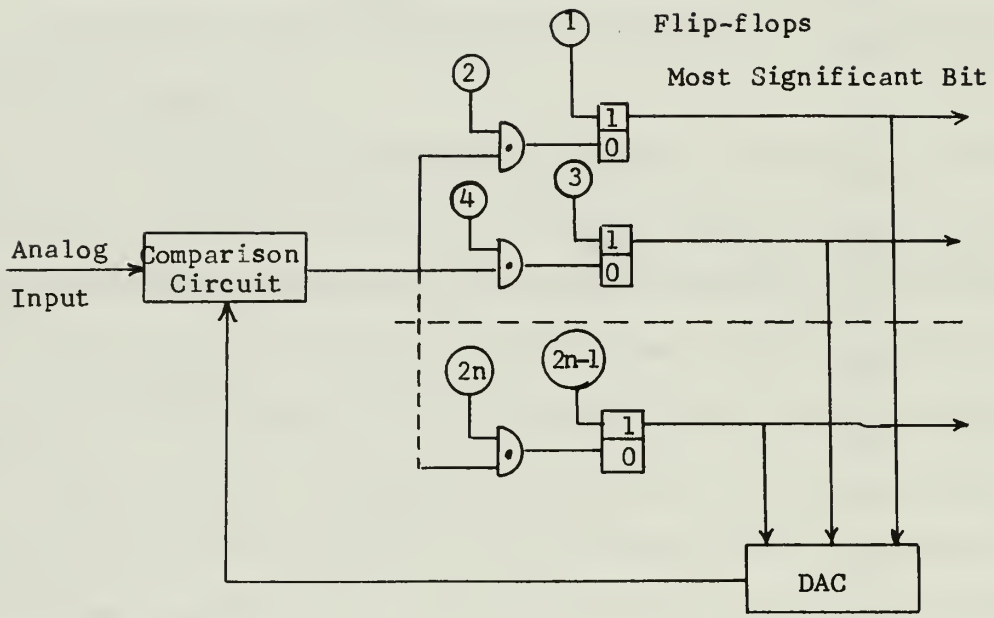


Figure 4.3. Coding by Successive Approximation

B. Time Base Encoding[2]

In this broad technique there are three problems that must be solved. These are the generation of an accurate reference voltage, the building of an accurate reference voltage, the building of a sensitive comparison circuit for comparing the reference signal to the signal to be coded, and the building of a counter which is capable of producing the coded value of the reference signal.

Utilizing the time base encoding principle there are presently three methods for achieving a digital representation of an analog quantity. The oldest and most common method utilites a linearly rising voltage (or staircase generator) as a reference voltage whereas more recent devices use either an exponential reference voltage or a sinusoidal reference voltage.

I. Staircase Reference Voltage. The method of operation is such that the voltage to be coded is compared with a linearly rising staircase voltage. As each step is generated the count increases by one. When the two voltages agree, the counting action stops and the contents of the counter are the coded representations of the input voltage. A diagram showing the operation is given in figure 4.4.

The conversion time for this type of converter depends on two factors; the counting rate r_c, of the counter, and the maximum number to be coded, P_{max}. The maximum conversion time = τ_{max}. [20]

$$\tau_{max} = \frac{P_{max}}{r_c} + \Delta \qquad (4.1)$$

[2]This title implies that a counter is used in conjunction with a source of precisely determined frequency to measure the time interval which elapses between two levels. [15]

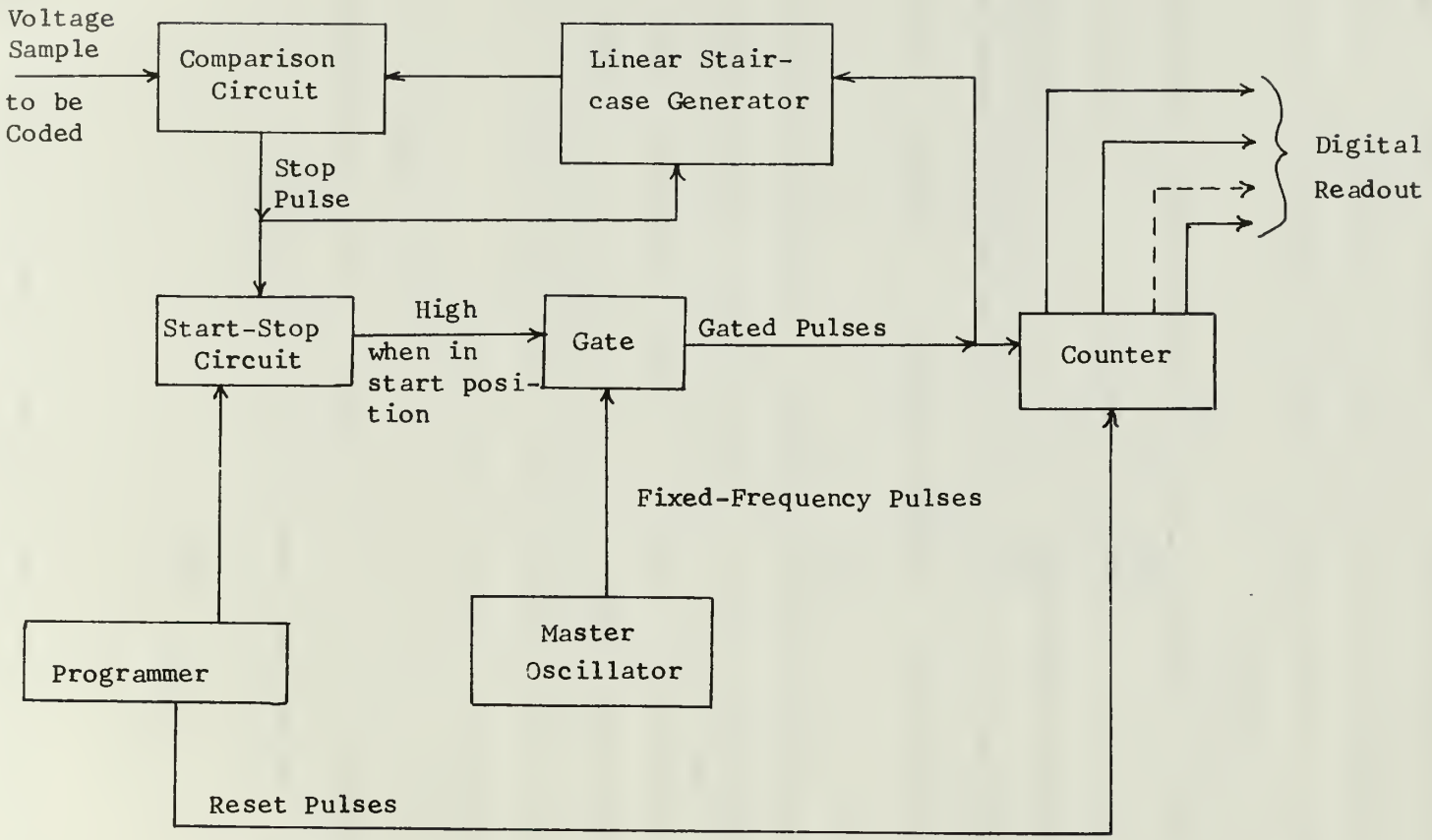


Figure 4.4. Coding by Intermediate Conversion to a Time Interval

where

$\triangle$ = time required to clear the counter. Usually this is of the order of 1 microsecond.

P_{max} = 1023 for the case of 10 bits required for encoding a three digit decimal number.

r_c = a typical figure is 20 megacycles per second at the present time.

$$\tau_{max} = \frac{1023}{20 \times 10^6} + 1 \times 10^{-6} = 51.1 \text{ microseconds/sample.}$$

This conversion time allows for approximately 20,000 samples or conversions per second. The voltage input levels to these converters range from 10 millivolts to 100 volts. [21]

The encoder can be time multiplexed with relative ease by sharing a great portion of the hardware as shown in figure 4.5.

II. Exponential Reference Voltage. Cronhjort (IRM Nordiska Laboratories) [22] has developed a time-base conversion encoding technique in which a decaying exponential voltage sweep is used. The sweep starts at the sampling instant, and "as the voltage declines it will at some instant reach a preset fixed reference level." [22] "During the time of decline the output of an oscillator of constant frequency is accumulated in a counter." [22] The pulse count accumulated represents a time interval which in turn is related to the input voltage at the sampling instant. The equation of the voltage sweep generated after a sampling has taken place is derived from figure 4.6.

$$u = (Au_X - u_b)\, e^{-t/\tau} + u_b \quad [22] \qquad (4.2)$$

where

u = input to comparator

u_b= biasing level of R-C tank circuit

Time Shared Components

Master Oscillator
Programmer
Linear Staircase Generator

MULTIPLEXING

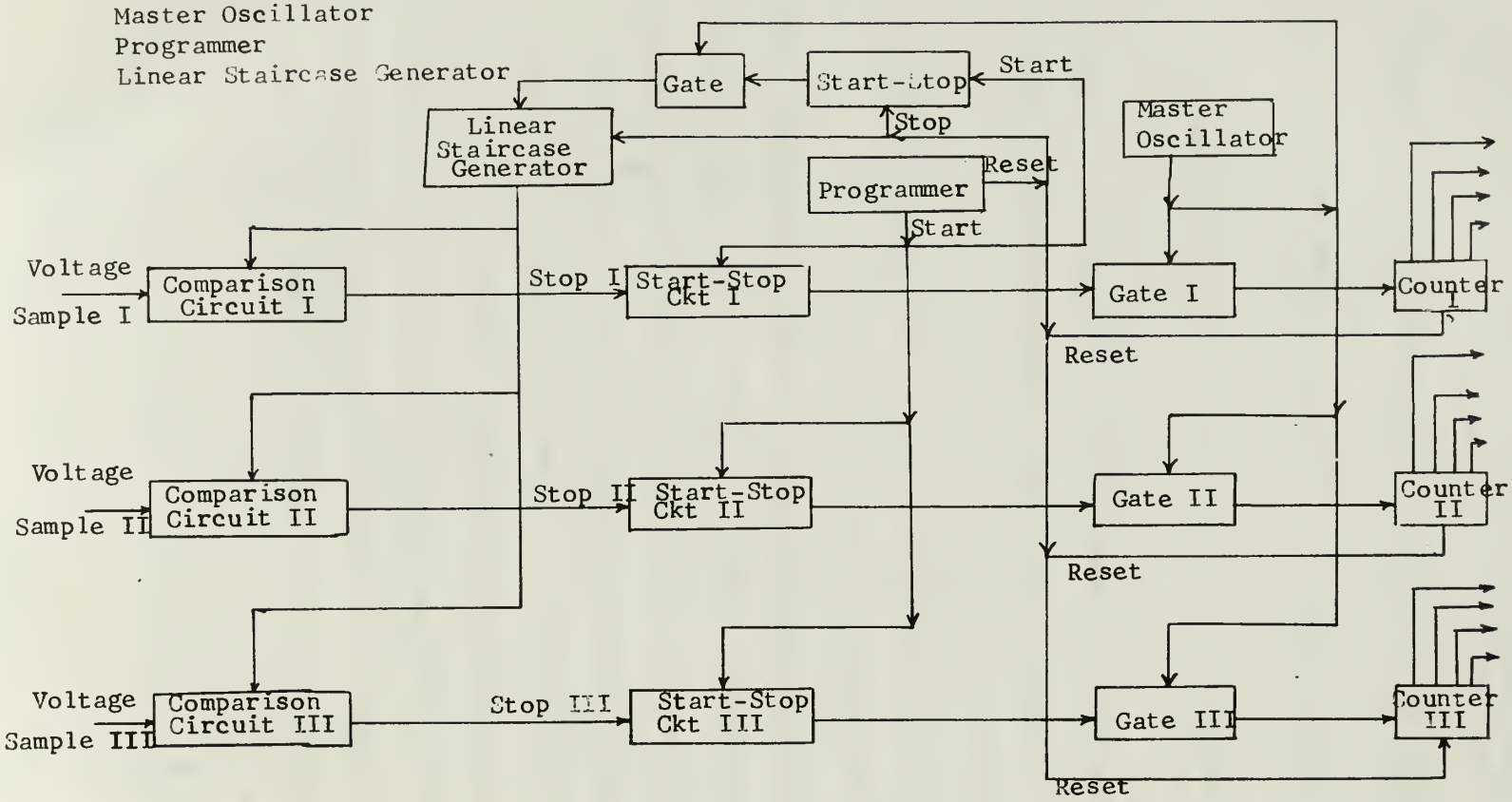


Figure 4.5. Multiplexing of the coding by Intermediate Conversion to a Time Interval Technique

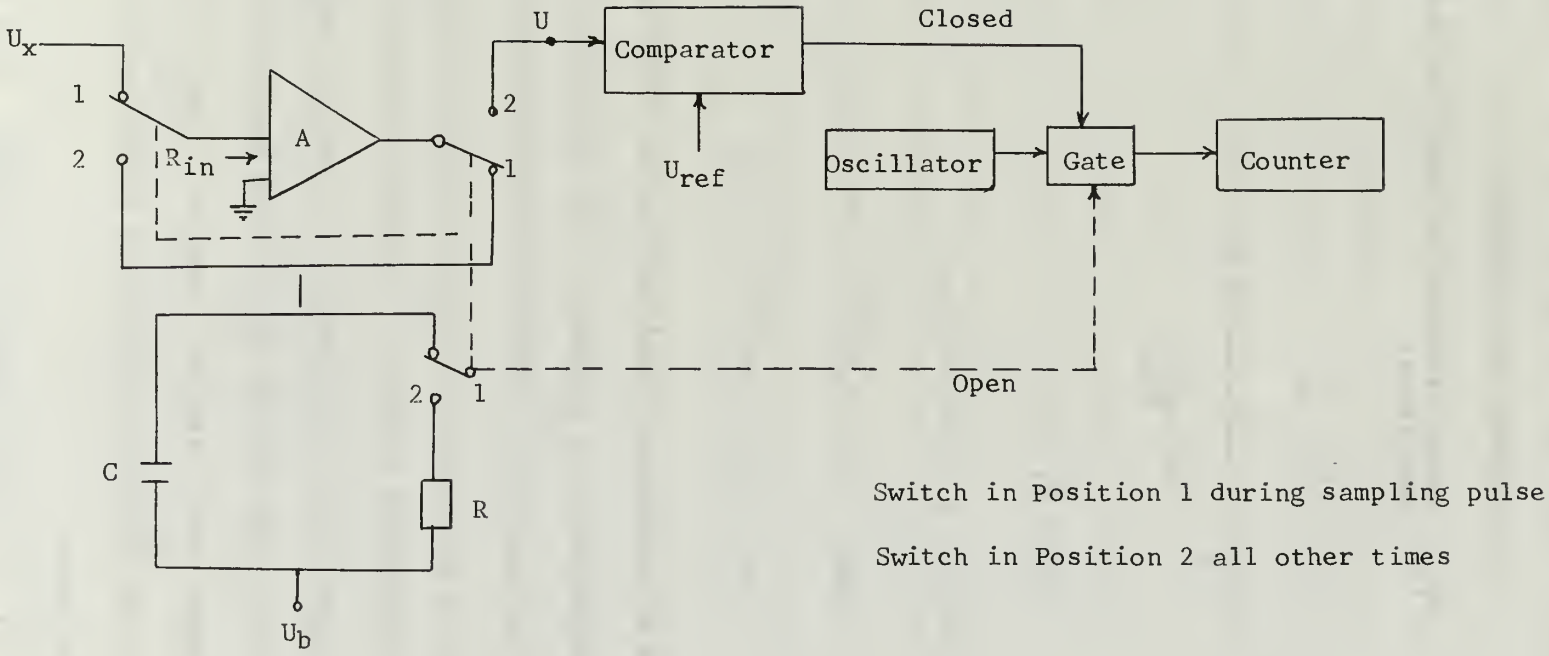


Figure 4.6. Time Base Encoding by Exponential Sweep

u_{ref} = reference voltage of comparator

τ = time constant of tank circuit

u_x = unknown input voltage

R_{in} = input resistance of amplifier A in figure 4.6 (assumed very large)

0 u_{ref} u_b.

$$R_d = \frac{R}{1 + \frac{R}{R_{in}}} = R \tag{4.3}$$

$$\tau = R_d \cdot C \tag{4.4}$$

Then at time t_1, u is set to u_{ref}

$$u_{ref} = (u_x - u_b)e^{-t_1/\tau} + u_b \tag{4.5}$$

$$u_x = (u_{ref} - u_b)e^{t_1/\tau} + u_b \tag{4.6}$$

Thus by measuring t_1 and solving Eq. (4.6) the unknown voltage u_x, can be determined by a computer. The exponential reference voltage method of conversion, in contrast to the staircase generator method, introduces a new concept to the conversion problem. This new idea is the use of a functional counter. In previous methods discussed the counter contents were linearly related to the voltage sweep, whereas in this case they are not, thus the use of the term functional must be included. Since it is assumed that a digital computer is part of the system the implementation of the solution of Eq. (4.6) can be carried out without any additional equipment.

III. Sinusoidal Reference Voltage. Mott [23] et. al. have proposed a new type of time base encoding. This type of encoding utilizes

a periodic (sinusoidal) reference voltage along with Cronhjort's idea of a functional counter. A block diagram of this type of encoding is given in figure 4.7 with three points depicted for waveform inspection and presentation as shown in figure 4.8. In this particular case of encoding, the functional counter is designed in such a fashion that clock pulses are accumulated from zero crossing, in positive going direction of the reference sinusoid up to the coincidence point of reference signal and analog input signal. The comparator circuit monitors the difference between the reference voltage and input voltage and produces an output when zero difference occurs as shown by waveform B in figure 4.8. This output signal inhibits the clock pulses and the counter content represents that coded value of the input analog signal at the sampling instant.

4.2. Digital-to-Analog. The purpose of this section is to discuss a type of DAC which is primarily used in feedback encoding ADC's. This type of converter is the operational amplifier connected as a voltage summer as shown in figure 4.9. The assumptions made for the derivation of the output voltage equation, in figure 4.9, are infinite gain and input impedance to the operational amplifier.[26] Then,

$$I_0 + I_1 + I_2 \ldots = I_f \tag{4.7}$$

$$\frac{E_{out}}{R_f} = - \frac{E_o}{2^o R_o} + \frac{E_1}{2^1 R_o} + \frac{E_2}{2^2 R_o} + \ldots \tag{4.8}$$

$$E_{out} = \frac{-R_f E_R}{R_o} (a_0 + a_1 + a_2 + \ldots + a_n) \frac{1}{2^n} \tag{4.9}$$

where the input voltages E_o, E_1, E_2, ... are obtained from switches which are connected either to the reference voltage E_R, or to ground depending on the bit setting. The output voltage E_{out} is a function of the binary

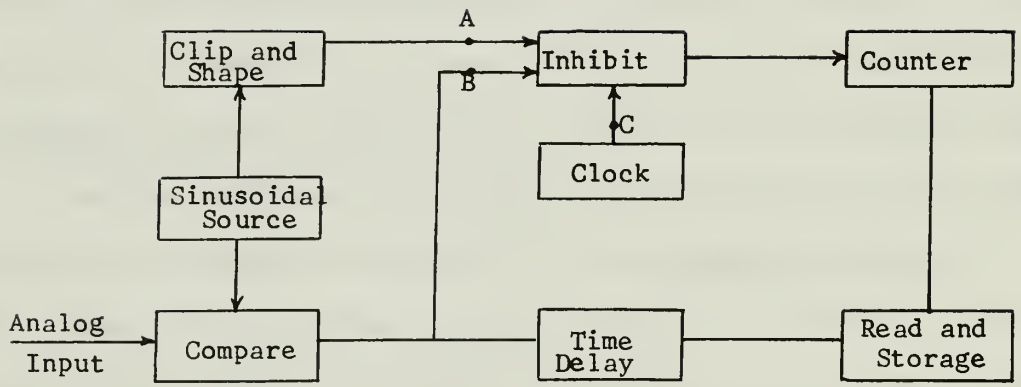


Figure 4.7. Time Base Encoding Using a Sinusoidal Reference Voltage

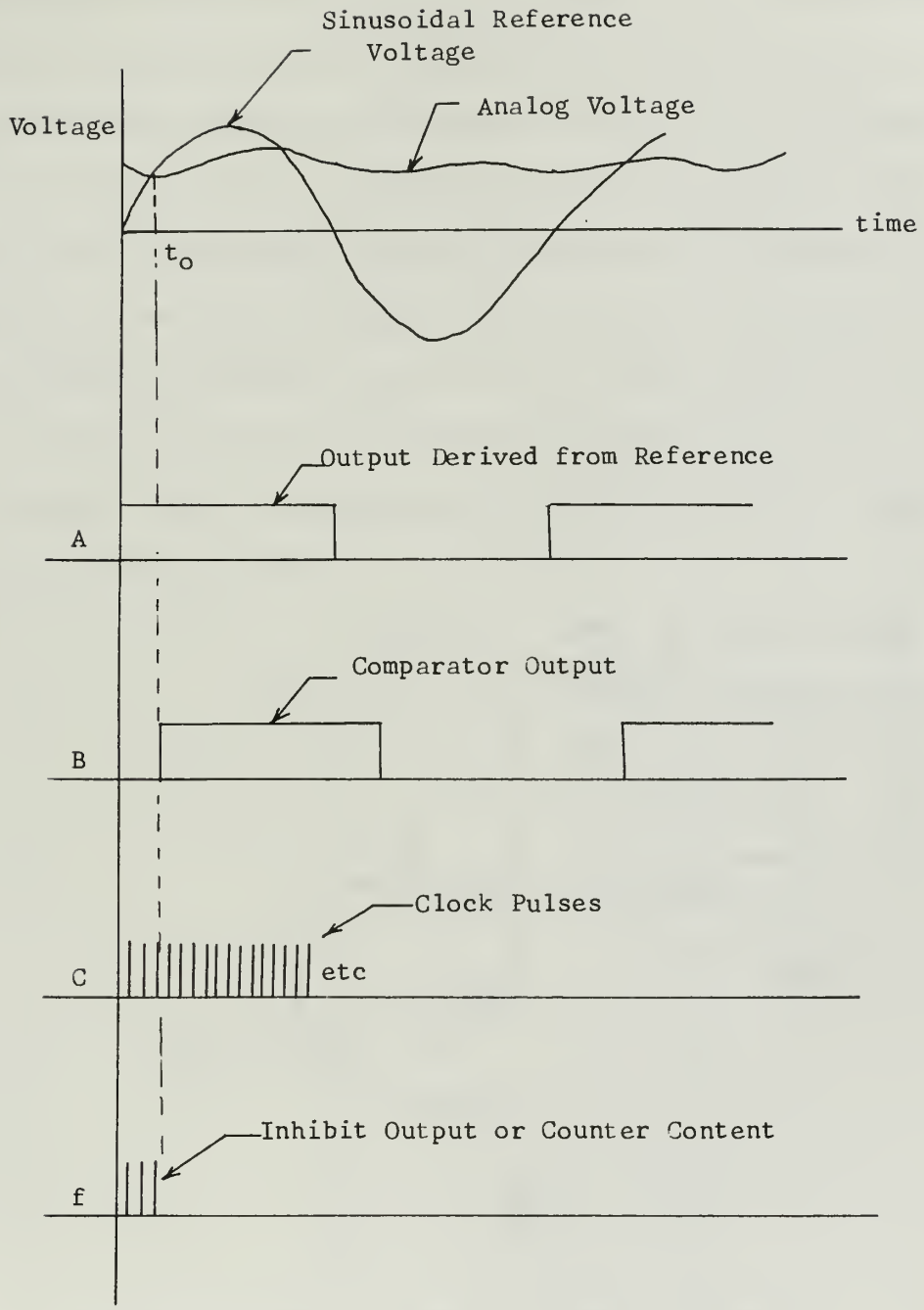


Figure 4.8. Waveforms at Several Points of Figure 4.7

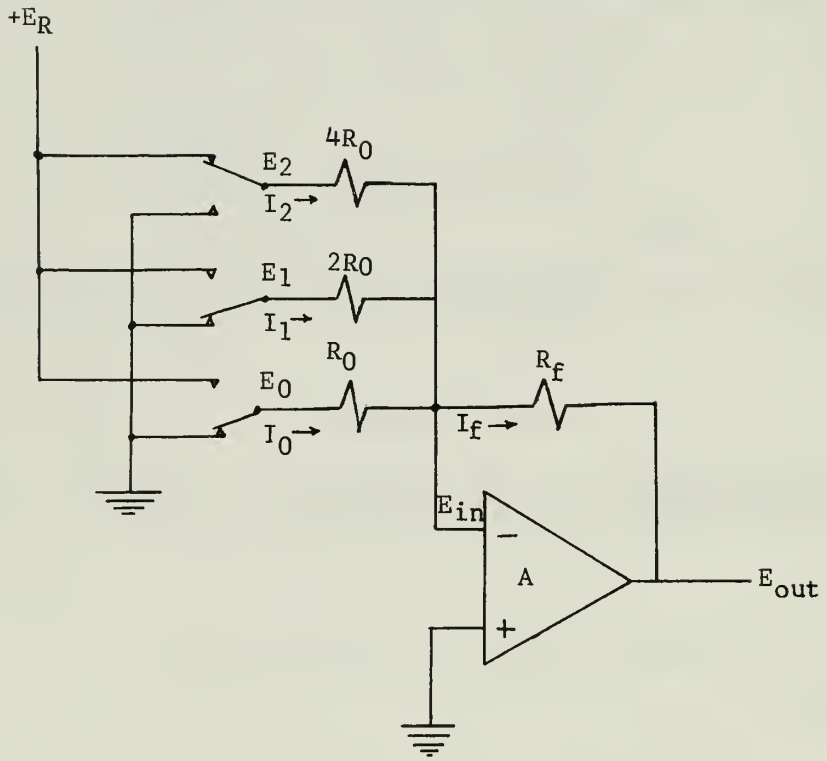


Figure 4.9. Ideal Operational Amplifier Connected as a Voltage Summer

number set on the switches, designated by a_o, a_1, a_2, $a_3 \cdots a_n$, where n is the number of bits and the a's are either 0 or 1. From Eq. (4.9) it is seen that the accuracy of voltage E_{out} is directly a function of the accuracy and stability of the feedback resistor, R_f, the summing resistors, (R_o, $2R_o$, $4R_o$, ... etc), and the reference voltage, E_R. High accuracy and stability power supplies are commercially available. [19] Rehn [17] has shown that the most critical resistors are R_f and R_o, whose tolerances must be 0.009% for the case of 11 bits, maximum allowable error of .05%. The tolerances on subsequent resistors ($2R_o$, $4R_o$, $8R_o$, etc) can be relaxed. This is shown below in Table 4.1 for Rehn's 11 bit DAC which had an error of 0.05%.

Table 4.1

Bit	Resistor	Maximum Allowable Error
a_o	2^0R_o	0.009%
a_1	2^1R_o	0.018%
a_2	2^2R_o	0.036%
a_3	2^3R_o	0.072%
a_4	2^4R_o	0.14%
a_5	2^5R_o	0.29%
a_6	2^6R_o	0.58%
a_7	2^7R_o	1.2%
a_8	2^8R_o	2.4%
a_9	2^9R_o	4.8%
a_{10}	$2^{10}R_o$	9.6%

Another source of error that is not obvious from Eq. (4.9), is the non-ideal characteristics of the switches used to set the binary digits. "These switches depart from ideal switches in that they have offset

voltage when 'on' and leakage currents when 'off.'" [19] An example of this is in Philco's ±10 volt DAC which utilizes semi-conductor DAC switch units. These switches have a maximum offset of 1 mv which result in an output error of 3.3 mv. [19] The assumption of infinite amplifier input impedance and gain does not cause any particular difference as can be illustrated from the following example.

Example 4. Amplifiers with voltage gain A, as shown in figure 4.9, ranging from 20,000 to 30,000 with a maximum output voltage of +10 volts are commercially available. [19]

$$E_{in} = \frac{10 \text{ volts}}{20{,}000} = 0.5 \text{ mv.}$$

The current flowing into the amplifier is E_{in} divided by the open loop input impedance of the amplifier = 25,000 ohms.

$$I_{in} = \frac{0.5 \text{ mv}}{25{,}000 \text{ ohms}} = 2 \times 10^{-8} \text{ amperes.}$$

From the foregoing discussion, it can be seen that the error in the DAC does not degrade the overall accuracy of an analog to digital converter of the type mentioned in the previous section.

5. Summary of Converter Characteristics

The analog-to-digital converters discussed have been classed into two basic categories: electromechanical and electronic.

The electromechanical converters normally have as an upper limit, sampling rates of approximately 400 samples/sec. Some of the encoding characteristics are summarized below in Table 5.1.

Table 5.1

Quantized Electromechanical Converter Characteristics

		Possibility of multiplexing external cktry	Code Conversion Required	Sample Available	Complexity of external circuitry
Coded Pattern	V-Brush Parallel	Yes	No	On Demand	Not simple
	Serial	Yes	No		Not simple
	V-Brush with self-switching	No external cktry required other than a bistable decision element	No		None required
	Gray Code	Yes	Yes		Not simple
Incremental Devices	Slotted Disc	No	No		Relatively Simple

The characteristics of electronic converters have a greater degree of divergence than do the electromechanical. The electronic converters are classed into three categories. These categories are listed below in Table 5.2 together with typical conversion rates.

Additionally, listed below in Table 5.3 are some analog-to-digital converters.

Table 5.2

Conversion Rates of Converter Techniques

Converter Type	Approximate Conversion Rate
Parallel	100,000-200,000 conversions/sec.
Successive Approximation	30,000-60,000 conversions/sec.
Time-base Encoding	20,000 conversions/sec.

Table 5.3

Electronic Converters

Towson Laboratories, Inc. (3500 Parkdale Ave., Baltimore, Md. 21211)

Model	No. Bits	Coding	Input	Sampling Rate	Accuracy
OC3100	8	Binary	±100mv & up	0-1200/sec	0.4% ±½ LSD
OC3100B	10	Binary	±0.5v & up	0-1000/sec	0.1% ±½ LSD
OC3101C-a	2	BCD	0 to +1 v	0-1200/sec	1.0% ±½ LSD
OC3101C-b	3	BCD	0 to +1 v	0-1000/sec	0.1% ±½ LSD
OC3101D-0	Bipolar	BCD	0 to ±0.5 v	0-920/sec	0.05% ±½ LSD
Airborne Models					
OC1001	10	Binary	±2.5 v	0-23,000/sec	0.15%
OC1501	10	Binary	0 to +5 v	0-25,000/sec	0.15%
High Speed					
OC2010A,B	8	Binary	0 to +1 v	0-185,000/sec	0.6%

Table 5.3
(continued)

Epsco Inc. (411 Providence Highway, Westwood, Mass. 02090)

Model	No. Bits	Coding	Input	Sampling Rate	Accuracy
Datrac 11	10,11,12, 13,14	Binary	0 to ±10 v	2 us/bit	.01% ±½ LSB
Video-verter	6	Binary	0 to ±10 v or -5v to +5 v	$10x10^6$ - 6 bit words/ sec	±½% of full scale ±½ LSB
AS-2	10	Binary	±5 volts	2 us/bit	±0.05% of full scale ±½ LSB

6. Applications in a Fuel Control System

This thesis has been primarily concerned with the discussion of various techniques of analog-to-digital conversion. This section is devoted to show how these interfacing techniques fit into a control system. The example selected is a turbine engine control system, as first presented by Goodfriend et. al. [24]

Turbine engine control is essential for the following reasons. The control system "(1) schedules fuel flow and other engine inputs to avoid compressor surge and turbine over-heating during acceleration, (2) prevents overspeeds and excessive turbine inlet temperature during steady state operation, and (3) prevents flameouts during decelerations." [24] In order to provide control for a turbine engine at all operating conditions, it is necessary to sense such parameters as compressor inlet pressure, burner section pressure, turbine inlet temperature, and engine speed. See figure 6.1 for locations where parameters must be sensed. Turbine inlet temperature cannot be sensed directly because a sensor which can operate continuously in temperature ranges upwards of 2000°F. has not been perfected. Thus it is necessary to combine some of the sensed parameters with engine characteristics to calculate turbine inlet temperature using thermodynamic equations. [24]

Engine control is accomplished by manipulating various engine input variables: [24]

(a) Gas generator fuel flow.

(b) Exhaust nozzle area.

(c) Compressor bleed valves.

(d) Inlet guide vanes.

(e) Compressor stator vanes, etc.

"Most fuel controls used on today's high performance gas turbine engines are of the hydromechanical type." [24] The controls operate on a preschedule basis, where the sensed parameter is compared to a reference parameter computed by the controller. [24] The calculation and storage of information is accomplished by mechanical linkages, variable orifices, cams, etc. Typical engine control schedules are shown in figure 6.2. A schematic of the Hamilton Standard JFC25 fuel control system is shown in figure 6.3. This type of a fuel control system is used extensively on commercial jet aircraft. [24] Hydromechanical control systems are efficient flight control devices but their adaptability to changes in control modes and schedule is not optimum. [24] It is desired that an adaptable system which can determine both engine requirements and optimum modes of control and schedules be incorporated. With this incorporation greater accuracy can be achieved than is presently possible with existing hardware. "This increase in accuracy will allow more effective engine development." [24]

With the above ideas in mind, Hamilton Standard designed and built a portable, flexible, digital electronic, real time control system. The digital electronic control system is divided into two sections: (1) On-line section, and (2) off-line section. The off-line section is used for system calibration and control mode checkout. The on-line control section is subdivided into three main parts; sensors, digital controller, and output devices.

Three categories of sensors are used in the on-line system.

(1) Twenty analog high level (0 to 5 volts) sensors are used for inputs such as pressure, rotary position, and selector switch positions. These inputs can be expanded to 40.

(2) Ten inputs are sensed by transducers which produce a

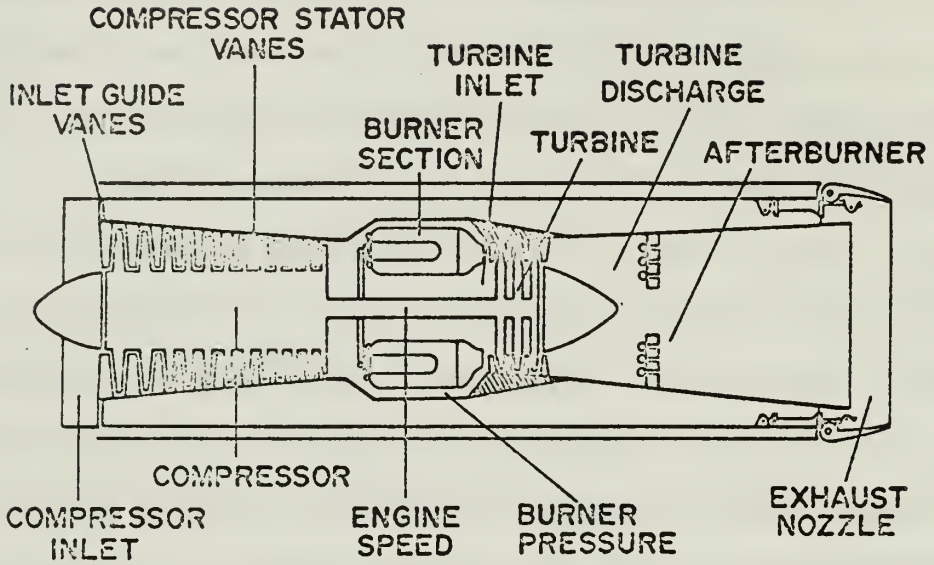


FIGURE 6.1 - TYPICAL AFTERBURNING TURBINE ENGINE

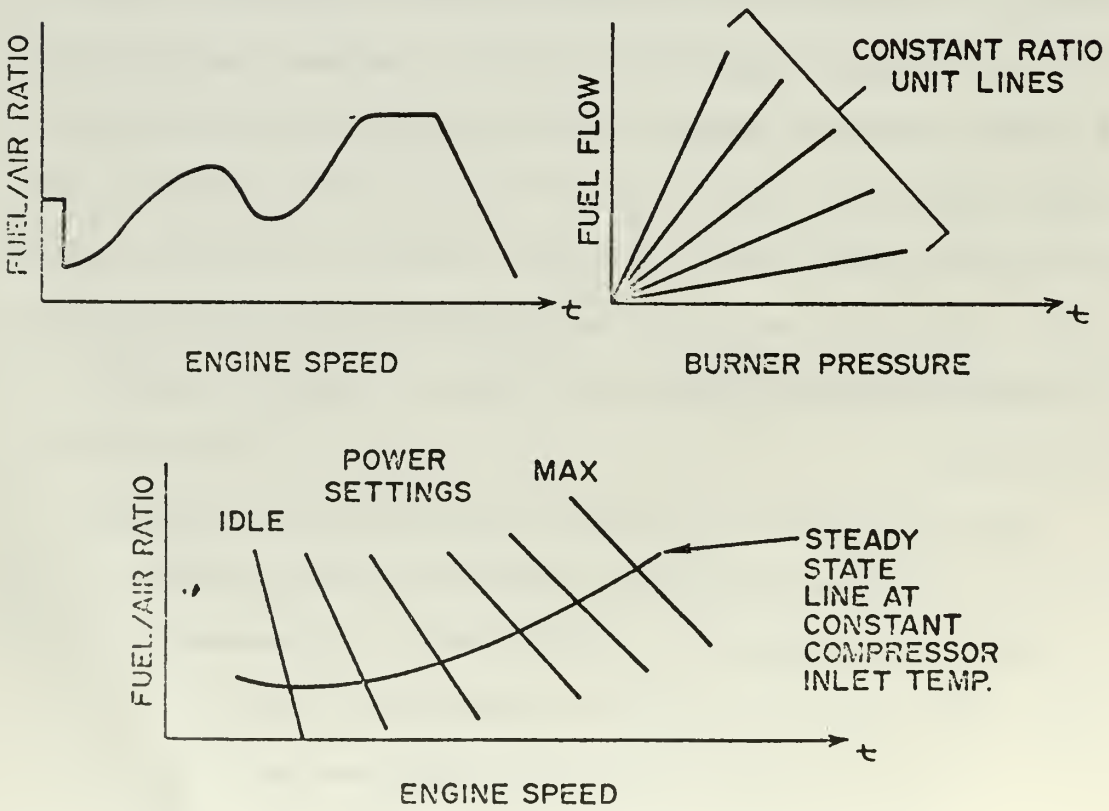


FIGURE 6.2 - TYPICAL GAS TURBINE ENGINE CONTROL SCHEDULES

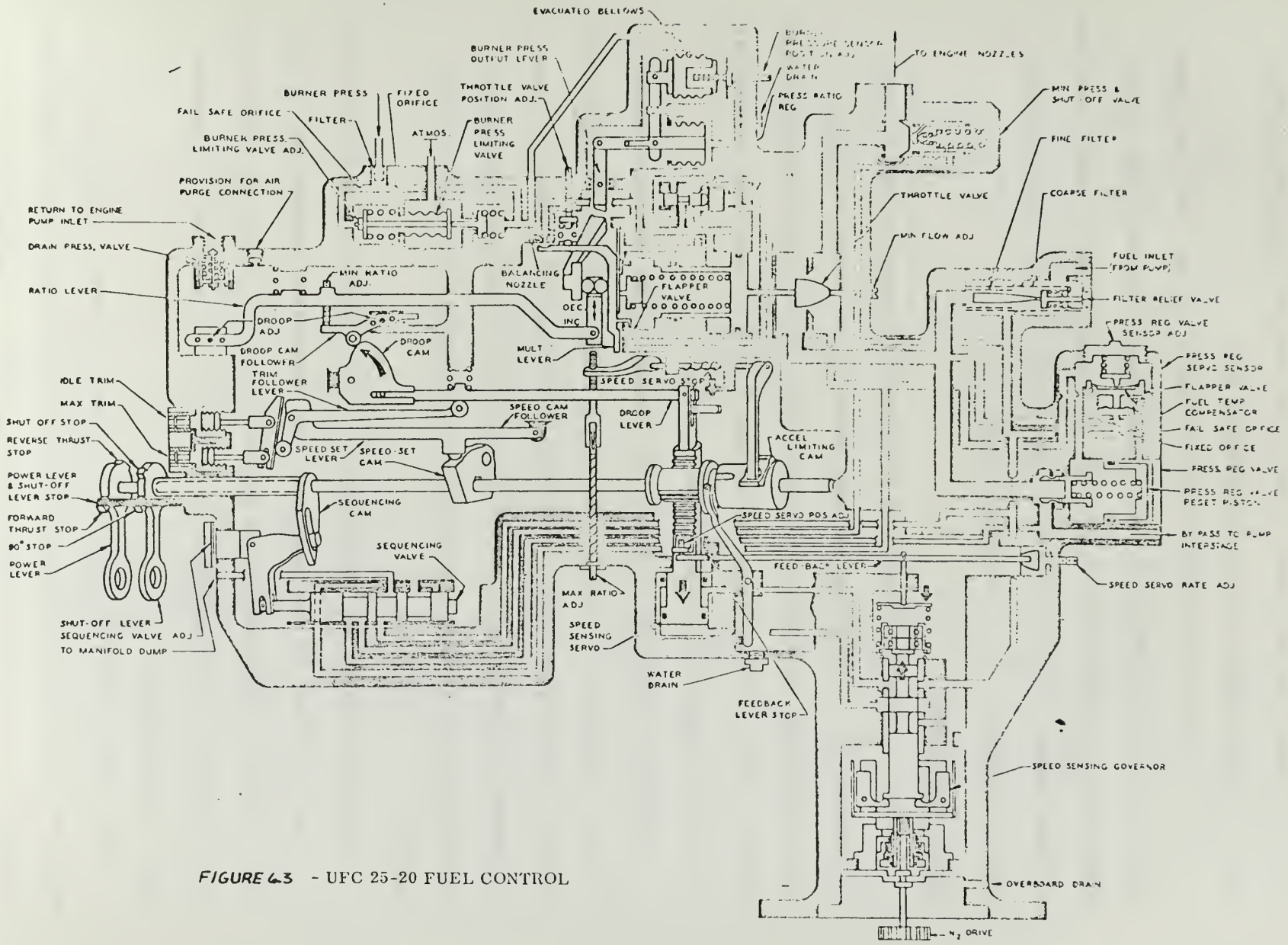


FIGURE 43 - UFC 25-20 FUEL CONTROL

frequency output proportional to the input such as fuel flow or rotor speed. These channels can be expanded to 20.

(3) Ten coded digital input channels are provided for inputs such as shaft positions, which determine power lever settings, or for other manually controlled parameters. The manual control panel consists of power lever, shut-off lever, and five shaft encoders with a 10-bit Gray code output. This is shown in figure 6.4.

System Operation

High level analog inputs are fed into the system through a multiplexer capable of accepting 20 input channels, as shown in figure 6.4. "The multiplexer sequentially transmits each of the analog inputs to the ADC at a rate of 200 readings per second." [24] The ADC then converts the 0 to 5 volt signal to a 16-bit binary number.

Frequency inputs are fed into the system in the separate channels. The input frequency is transformed into a pulse, and then through a period gate. The period "gates" a ten or five megacycle counter in order to provide a count proportional to the period of the input frequency. The binary count is then transferred to the computer through a buffer register.

Gray code inputs are fed through a multiplexer, to a Gray-to-binary converter, and then to the computer. The controller outputs are in two forms: analog currents which are proportional to a binary bit setting and switch closures for solenoid actuated devices. Output data is updated every 5 milliseconds.

The analog acquisition units, as shown in figure 6.6, consist of a high level multiplexer, sample and hold circuit, and a 13-bit binary ADC. The ADC is a successive approximation type with a resolution of 2^{-13}. A

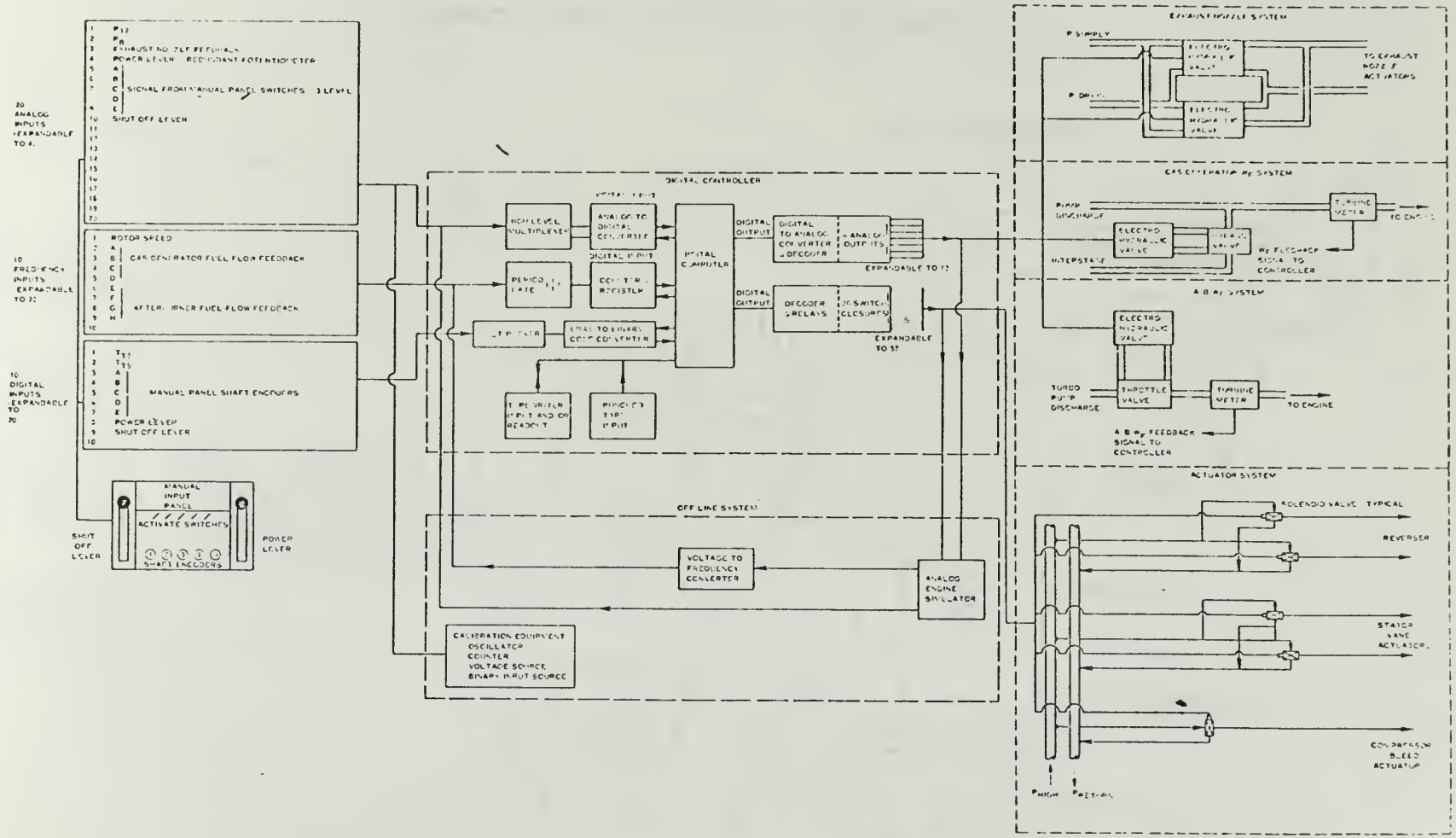


FIGURE 6.4 - HAMILTON STANDARD DIGITAL ELECTRONIC BREADBOARD

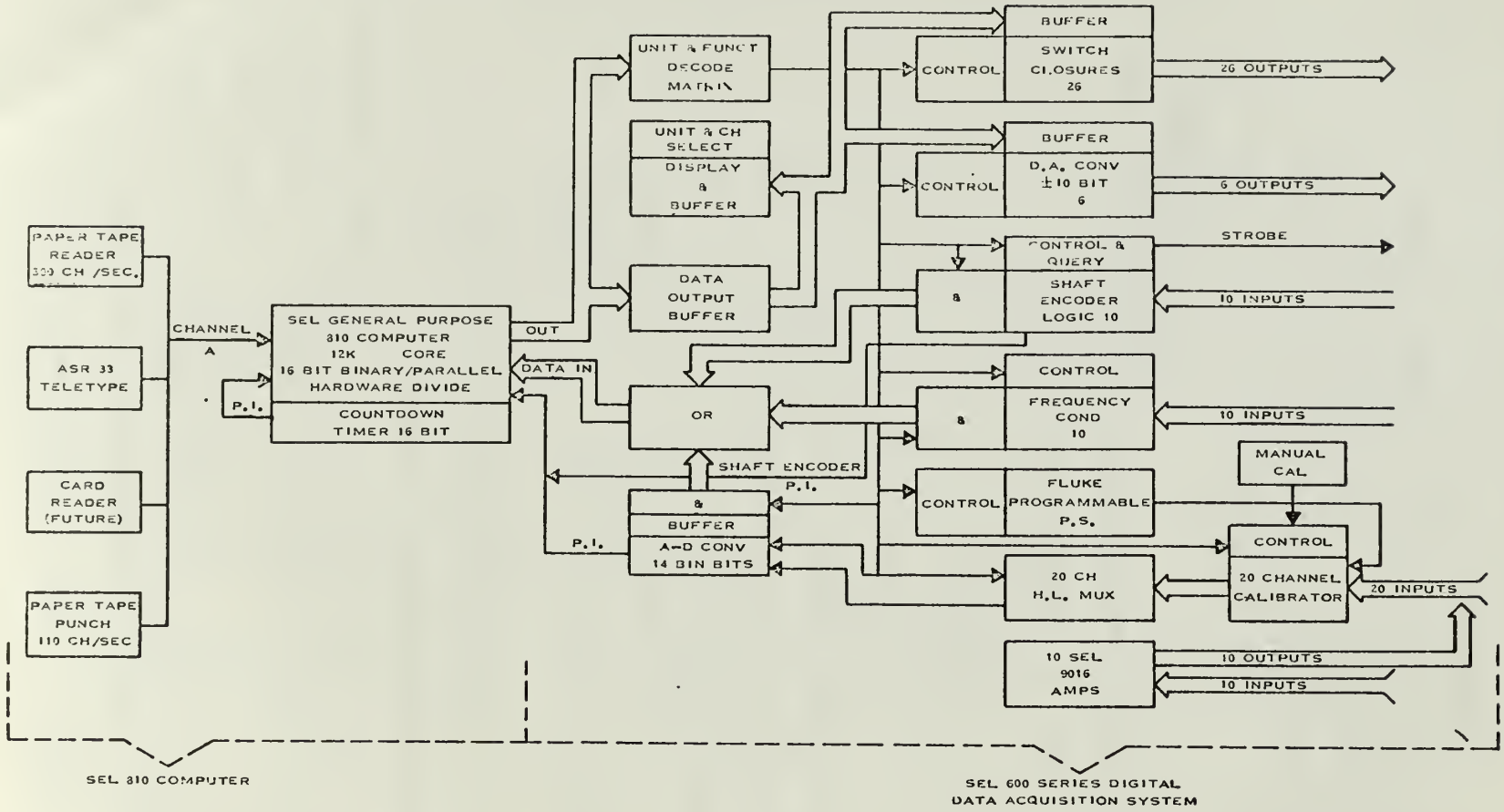


FIGURE 6.5 - TYPICAL CONTROLLER BLOCK DIAGRAM

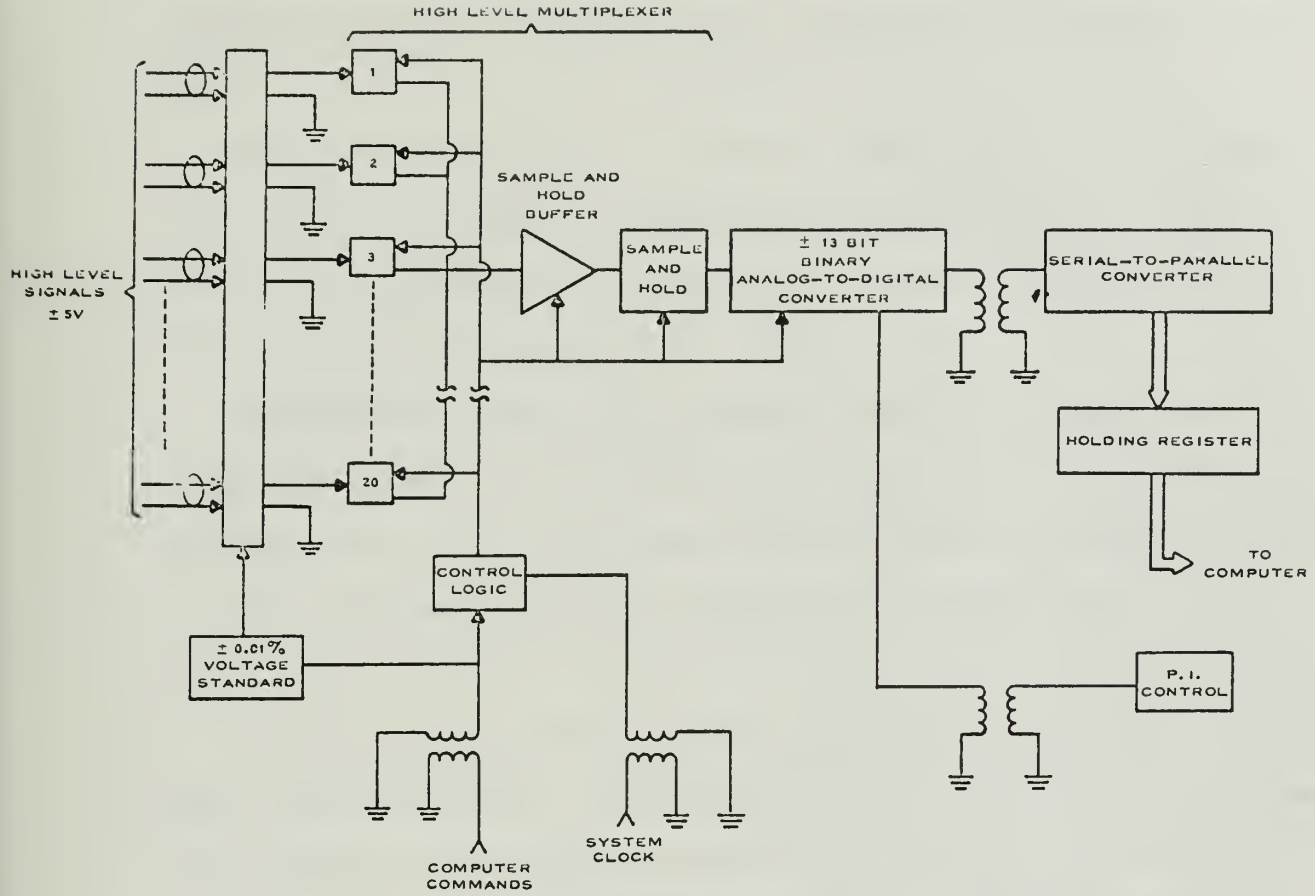


FIGURE 6.6- ANALOG ACQUISITION BLOCK DIAGRAM

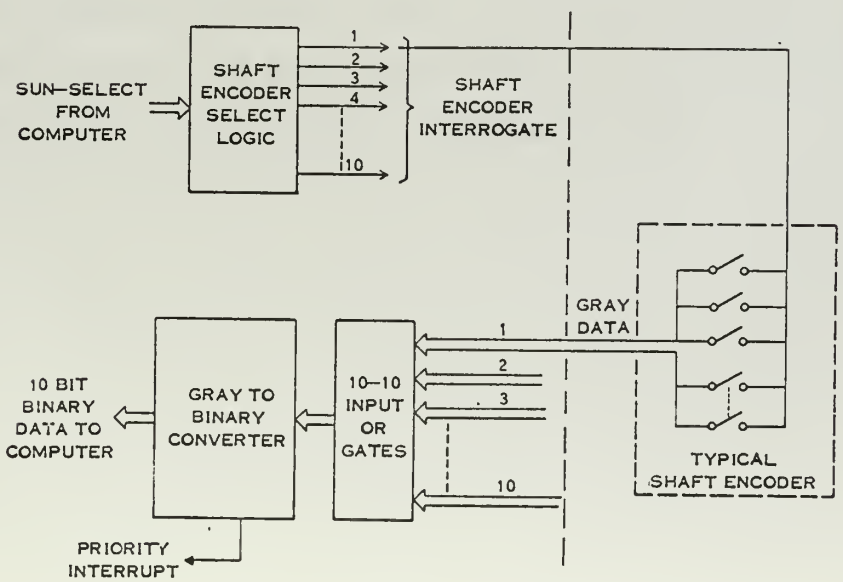


FIGURE 6.7 SHAFT ENCODER INPUT LOGIC

sample and hold circuit is incorporated at the input to the ADC. The sampling process has an aperture time (sampling pulse width) of 1 microsecond.

The shaft encoder inputs, as shown in figure 6.7, are 10 bit Gray coded inputs which must be converted to straight binary code. This conversion is done outside of the computer. A common Gray-to-binary conversion circuit is used for all ten inputs.

The DAC's are used as output current sources. The DAC's convert a 10 bit digital word into its proportional current level. Each DAC holds its output level until a new digital value is received from the computer.

The controller performance capabilities are given below in Table 6.1.

The fuel control system just discussed operates at relatively high speeds (200 samples/sec). This performance requirement may be contrasted with a typical process control system in which sampling intervals for flow variables are of the order of magnitude of 1 second, pressure variable of the order of 5 seconds, and temperature variable of the order of 10 seconds. [25] These slower processes and sampling rates allow for convenient time sharing of the computer. In fact, control of upwards of 200 control loops have been accomplished. [25]

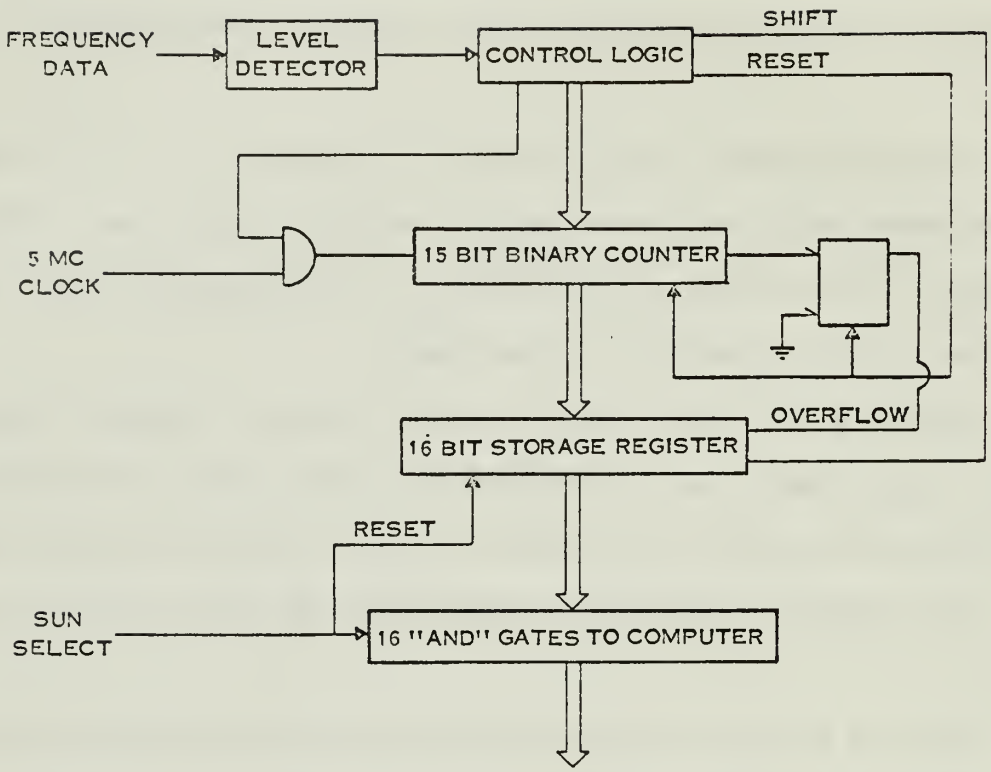


FIGURE 6.8 - FREQUENCY CONDITIONER LOGIC

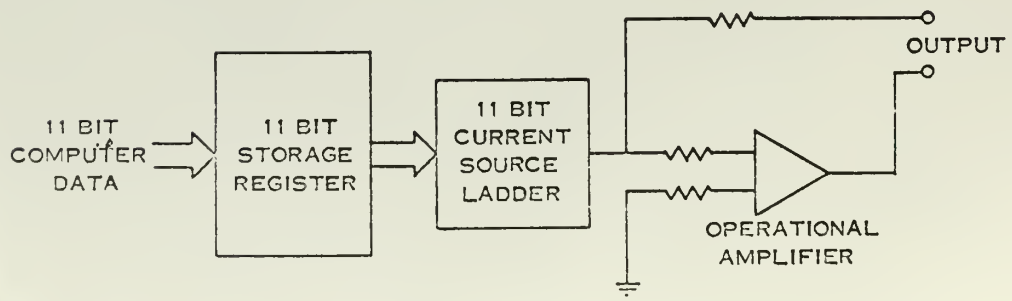


FIGURE 6.9 - DIGITAL TO ANALOG CONVERTER

Table 6.1

Controller Performance

High-Level Multiplexer	
Full scale input	±5.00 volts
Input impedance	500,000 ohms
DC Linearity	±0.005% best straight line
Gain stability	±0.0005%/°F
Zero drift	±0.007%/°F
Offset	±0.005% FS (full scale)
Analog-to-Digital Converter	
Linearity	±0.01% FS
Zero drift	±0.002%/°F
Gain stability	±0.001%/°F
Quantizing error	½ LSB
Frequency Signal Conditioner	
Local Oscillator Frequency	10 MC ±0.001%
Oscillator Output Stability	1×10^{-8}/24 hours
Period Counter Error	± 1 microsecond
Input Period Range	150 to 18,000 PPS channels 1 through 8 300 to 18,000 PPS channels 9 and 10
Shaft Encoder	
Number of Converters	10
Number of Bits	10
Conversion Time	100 microseconds

Table 6.1
(continued)

Digital-to-Analog Converters

Number of converters	6
Output	± 20 milliamperes into 1K load
Accuracy	± 0.5% FS
Resolution	± 10-bit binary
Type output	Current source

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APPENDIX A

Codes

The purpose of this Appendix is to list some of the other codes that may be used in analog to digital conversion. Some of these codes may be used for error checking, error correcting, or to prevent ambiguities from occurring. These are listed in Tables 1 through 4 of this Appendix.

TABLE 1

(BASIC BINARY)

Decimal	Straight Binary	Reflected Binary [13]	Binary Coded Decimal
0	0000	0000	00000
1	0001	0001	00001
2	0010	0011	00010
3	0011	0010	00011
4	0100	0110	00100
5	0101	0111	00101
6	0110	0101	00110
7	0111	0100	00111
8	1000	1100	01000
9	1001	1101	01001
10	1010	1111	10000
11	1011	1110	10001
12	1100	1010	10010
13	1101	1011	10011
14	1110	1001	10100
15	1111	1000	10101

TABLE 2

(NON-BINARY CODES)

Decimal	Octal	Reflected Octal [13]	Quaternary	Reflected Quaternary [13]
0	0	0	0	0
1	1	1	1	1
2	2	2	2	2
3	3	3	3	3
4	4	4	10	13
5	5	5	11	12
6	6	6	12	11
7	7	7	13	10
8	10	17	20	20
9	11	16	21	21
10	12	15	22	22
11	13	14	23	23
12	14	13	30	33
13	15	12	31	32
14	16	11	32	31
15	17	10	33	30
16	20	20	100	130

TABLE 3

(WEIGHTED BINARY CODES) [5]

Decimal	5,4,2,1	2,4,2,1	5,3,1,1	7,4,-2,-1
0	0000	0000	0000	0000
1	0001	0001	0001	0111
2	0010	0010	0011	0110
3	0011	0010	0100	0101
4	0100	0100	0101	0100
5	1000	1011	1000	1010
6	1001	1100	1001	1001
7	1010	1101	1011	1000
8	1011	1110	1100	1111
9	1100	1110	1101	1110

TABLE 4

(Excess 3 Code) = (Binary representation of D + 3) [5]

Decimal	Excess 3
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

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13. ABSTRACT

This thesis is primarily concerned with a comparative study of analog-to-digital conversion techniques as currently available. Those discussed and evaluated are of the electromechanical and electronic types including coded patterns, incremental devices, simultaneous, feedback encoding, and time base conversion. In addition to the study of converter techniques and characteristics the last section is devoted to a practical application for a turbine engine fuel control system. Numerous tables and charts for purposes of comparison are included.

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	ROLE	WT	ROLE	WT	ROLE	WT
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Conversion						
Converters						
Control Systems						
Digital Control						

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